IEEE
ELECTRON DEVICES SOCIETY
Newsletter

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BoG Meeting Recap and New EDS President Elect!

The EDS Board of Governors (BoG) meeting series was held in conjunction with the 2013 International Electron Devices Meeting (IEDM) in Washington, DC. The BoG series was particularly spirited this year, with over a dozen committee and ancillary meetings taking place during the weekend of December 6–8.

EDS is blessed with a diverse and engaged volunteer corps charged with stewarding the society's vital interests in all areas of our operations: conferences, publications, membership engagement, technical activities and education. The BoG meeting was especially lively this year, with over 20 volunteers presenting.

Among the major actions taken was the BoG approval of revisions to the EDS Constitution and Bylaws. Led by an Ad-hoc committee comprised of BoG members Simon Deleonibus (Chair), Cor Claeys, Jacobus Swart, and Zeynep Celik-Butler, and with assistance from Irv Engelson, the changes to EDS's governing documents will provide better consistency, transparency, and flexibility into EDS's structure and operations. The revised

(continued on back cover)

2014 IEEE Photovoltaic Specialists Conference (PVSC)

RICH GRANT AND VISIT DENVER

Denver skyline from City Park Golf Course

We invite you to join us for the 40th IEEE Photovoltaic Specialists Conference (PVSC), being held June 8–13, 2014, in Denver, Colorado. Since our first meeting in 1961, the PVSC has established itself as the world's leading technical event for scientists, engineers and decision-makers across the full spectrum of PV technologies.

As PV technologies continue to leap forward at an unprecedented pace, we are expecting yet another tremendous conference. Here are just some of the highlights to come.

40th IEEE PVSC Highlights

Tutorials

As always, the week will begin with a series of educational sessions on PV technologies and markets. These half-day tutorials will offer valuable insights for everyone from industry newcomers who may appreciate the "Photovoltaics 101" sessions, to veterans looking to expand their understanding in new areas, such as Si experts

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Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at radhakrishnan@ieee.org

ELECTRON DEVICES SOCIETY

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EDS Board of Governors (BoG)
Elected Members-at-Large
Elected for a three-year term (maximum two terms) with 'full' voting privileges

2014	Term	2015	Term	2016	Term
Z. Celik-Butler	(1)	Daniel Camacho	(1)	A. Escobosa	(2)
M. Chan	(1)	Subramanian S. Iyer	(2)	Ru Huang	(1)
S. Chung	(1)	Meyya Meyyappan	(2)	Leda Lunardi	(1)
S. Deleonibus	(2)	Arokia Nathan	(2)	M. Ostling	(2)
F. Guarin	(2)	Michael Shur	(2)	M.K. Radhakrishnan	(2)
T.L. Ren	(1)	Doug Verret	(1)	Jacobus Swart	(1)
S. Saha	(2)	Bin Zhao	(2)	X. Zhou	(2)
E. Sangiorgi	(1)				

NEWSLETTER EDITORIAL STAFF

Contributions Welcome

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either the Editor-in-Chief or appropriate Editor. The e-mail addresses of these individuals are listed on this page. Whenever possible, e-mail is the preferred form of submission.

Newsletter Deadlines

Issue	Due Date
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at http://eds.ieee.org/eds-newsletters.html. The archive contains issues from July 1994 to the present.

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Upcoming Technical Meetings

2014 IEEE International Vacuum Electronics Conference (IVEC)

We are pleased to announce that the Fifteenth International Vacuum Electronics Conference (IVEC 2014) will be held April 22–24, 2014, at the Portola Hotel & Spa in Monterey, California. Visitors from around the world come to Monterey to experience its natural coastal beauty, visit the renowned Monterey Bay Aquarium, and experience its rich historic past memorialized in the novels of John Steinbeck.

With technical co-sponsorship from the IEEE Electron Devices Society, the conference will provide a forum for scientists and engineers from around the globe to present the latest developments in vacuum electronics technology at frequencies ranging from the UHF to THz bands.

IVEC was originally created in 2000 by merging the U.S. Power Tubes Conferences and the European Space Agency TWTA Workshops. Now a fully international conference, IVEC is held every other year in the U.S., and in Europe and Asia alternately every fourth year. After the successful and enjoyable meeting in Paris, France in May, IVEC 2014 will return to its beautiful U.S. location in the city of Monterey.

Plenary talks will provide insights into the history, the broad spectrum of fundamental physics, the scientific issues, and the technological applications driving the current directions in vacuum electronics research. Technical presentations will range from the fundamental physics of electron emission and modulated electron beams to the design and operation of devices at UHF to THz frequencies, theory and computational tool development, active and passive components, systems, and supporting technologies. System developers will find that IVEC provides a unique snapshot of the current state-of-the-art in vacuum electron devices. These devices continue to provide unmatched power and performance for advanced electromagnetic systems, particularly in the challenging frequency regimes of millimeter-wave and THz electronics.

The John R. Pierce Award for Excellence in Vacuum Electronics and a Student Paper Award will be presented at the conference. As in past conferences, the meeting and social events will provide unique opportunities to renew or establish new friendships with colleagues, interact with customers and end-users, and meet students and academic researchers.

The conference website is the best source of information about IVEC 2014, including Technical Areas, Paper Submission, Registration, Accommodation, and other important dates and events. Please visit http://ivec2014.org/. To enquire about exhibitor space and conference support, contact Alicia Waldron, Palisades Convention Management (212-460-8090 ext. 216, awaldron@pcm411.cm).

You also can learn more about IVEC by visiting http://vacuumelectronics.org/, the EDS Vacuum Electronics Technical Committee website.

We look forward to seeing you in Monterey!

David K. Abe
2014 IVEC General Chair
U.S. Naval Research Laboratory
Washington, DC, USA

2014 IEEE International Reliability Physics Symposium (IRPS)

The IEEE International Reliability Physics Symposium (IRPS) is the world's premier forum for leading-edge research addressing developments in the Reliability Physics of devices, materials, circuits, and products. IRPS is the conference where emerging Reliability Physics challenges and possible solutions to achieve realistic End-of-Life projections are first discussed. This year, the IRPS will be held at Hilton Waikoloa Village, Waikoloa, HI, U.S.A. Scheduled for June 1–5, 2014, the IRPS will commence with two full days of tutorials and year-in-review on Sunday, June 1st and Monday, June 2nd.

The IRPS draws presentations and attendees from industry, academia and governmental agencies worldwide. No other meeting presents as much leading work in so many different areas of reliability of electronic devices, encompassing silicon device, non-silicon device,

process technology, nanotechnology, optoelectronics, photovoltaic and MEMS technology.

For the IRPS 2014, we are emphasizing Electronic Systems reliability with sub-topics in consumer electronics reliability and design-for-reliability. We are also emphasizing chip-package interactions and advanced packaging reliability concerns.

IRPS 2014 will also feature increased participation in the fields of Advanced CMOS scaling, GaN, new materials introduction, new processes or integration strategies, and/or fundamentally new device architectures. The conference will offer a full slate of tutorials, evening panel debates and workshops, invited plenary talks in addition to an outstanding technical program.

The hotel is located in Waikoloa Village on the Island of Hawaii (known as The Big Island). It has a wide variety of resort activities to choose from and is the perfect starting point to explore Hawaii Island, the Island of Adventure. At the Waikoloa resort, there are endless opportunities including interactive dolphin encounters, snorkeling, kayaking, and standup paddle boarding. Also, there are two championship golf courses within the Waikoloa Beach Resort. Several guided tours to Volcano National Park, Mauna Kea summit and Waipio Valley are available. You can view the video of the resort on IRPS website www.irps.org

IRPS consists of three days (Tues–Thurs, June 3–5) of plenary and parallel technical sessions presenting original, state-of-the-art work.

Other opportunities at the symposium include:

At the resort, there are endless recreation opportunities, including interactive dolphin encounters, snorkeling, kayaking, standup paddle boarding and fun in one of three pools with water slides and waterfalls. (Photos courtesy of Hilton Waikoloa Village).

- Two-Day **Tutorial Program** (Sunday–Monday, June 1–2). The IRPS tutorial program is a comprehensive two-day event designed to help both the new engineer and experienced researcher. The tutorial program contains both beginner and expert tracks, and is broken down into topic areas that allow the attendee to participate in tutorials relevant to their work with a minimum of conflicts between subject areas.
- **Year in Review Session** (Monday, June 2). These seminars provide a summary of the most significant developments in the reliability community over the past year. This serves as a convenient, single source of information for attendees to keep current with the recent reliability literature. Industry experts serve as the "tour guide" and save you time by collecting and summarizing this information to bring you up to date in a particular area as efficiently as possible.
- **Poster Session** will provide an additional opportunity for authors to present their original research. The setting is informal and allows for easy discussion between authors and other attendees.
- **Panel Discussion and Workshop Sessions** enhance the symposium by providing the attendees an opportunity to hear the thoughts and opinions of industry experts and meet in informal groups to discuss key reliability physics topics with the guidance of experienced moderators. Some of the workshop topics are directly coupled to the technical program to provide a venue for more discussion on the topic.
- **Vendor Exhibits**. Held in parallel with the technical sessions, the equipment demonstrations provide a forum for manufacturers of state-of-the-art laboratory equipment to present their products. Attendees are encouraged to visit the manufacturers' booths for information and demonstrations.
- **IRPS Paper Awards**. IRPS bestows awards for Best Paper, Outstanding Paper, Best Poster and Best Student Talk. The Best Paper author is typically invited to present the paper at ESREF in October.

For registration and other information, visit the IRPS 2014 home page at http://www.irps.org/ .

The IRPS committee members look forward to seeing you in June.

Charles Slayman
2014 IRPS Publicity Chair
Cisco Systems

Prasad Chaparala
2014 IRPS General Chair
Alta Devices

2014 IEEE International Interconnect Technology Conference (IITC)/Advanced Metallization Conference (AMC)

The 17th annual IITC conference will be held May 21–23, 2014, in conjunction with the 31st Advanced Metallization Conference at the DoubleTree Hotel in San Jose, California. It will be preceded by a day-long workshop on "**Manufacturing of Interconnect Technologies: Where are we now and where do we go from here?**" on Tuesday, May 20th. The conference attracts professionals from industry, academia, and national laboratories in semiconductor processing, interconnect design, and equipment development.

Recognizing the industry's need to look at disruptive interconnect solutions in the long term, the conference will feature sessions dedicated to advanced materials, such as carbon-based interconnects, atomic layer deposited dielectrics and atomic layer deposited metals. Other important topics for IITC/AMC 2014 include dielectric reliability, 3D integration as well as design and architectural solutions to interconnect challenges.

IITC/AMC 2014 continues to address fundamental interconnect performance issues, with presentations in the areas of process integration (for logic and/or memory); reliability; advanced interconnects and systems interconnections; through-silicon vias and 3D integration; packaging; novel materials and concepts; process modeling, and all back-end materials and unit processes associated with interconnect technology, including in-depth explorations of related manufacturing issues.

The IITC rotates its location between Asia, the US, and Europe. In 2013, IITC was held in Kyoto, Japan. In 2012, IITC was held in San Jose. The 2015 IITC will be held in Europe. Oral and poster presentations at IITC/AMC 2014 will include the following topics:

Materials and Unit Processes

- Dielectric materials and associated deposition
- Metal deposition, planarization and patterning processes/equipment
- Novel or improved tools for interconnect metrology

Novel Materials and Concepts

- Carbon based interconnects, including vias and interconnects composed of carbon nanotubes or grapheme
- Optical interconnects and RF interconnects

3D Integration
- Through silicon via (TSV) materials, process integration, reliability, interactions with packaging
- 3D packaging schemes
- Circuits and architecture for 3D integration

Process Integration and Chip Package Interactions
- Multilevel interconnect processes, novel interconnect structures, contact/via integration, metal barrier and materials interface issues
- Integration processes and issues specific to logic or memory
- Novel non-volatile, interconnect embedded memories

Process Modeling
- CMP, metal/dielectric deposition and etching processes

Reliability
- Metal electromigration and stress voiding, dielectric integrity, thermal effects, passivation issues, interconnect reliability prediction/ modeling.

Memory Materials in the Interconnect
- Memory Materials like Phase Change Memory (PCM), Resistive RAM (RRAM), Conductive Bridge RAM (CB-RAM) and Magnetoresistive RAM (MRAM)

Interconnect Systems
- Interconnect performance modeling and high frequency characterization
- Interconnect system integration, novel architectures and advanced interconnect concepts
- Circuit techniques to improve interconnects

Novel Systems and Packaging
- Wafer-level packaging schemes
- Packaging of optical interconnects, RF, and SoC

Contacts and Front-end Metallization
- Salicides, replacement gate processes, local interconnects

Supplier Exhibits and Seminars

Supplier exhibits and seminars are included as an integral part of the IITC/AMC technical program. Held on the first and second days of the conference, the supplier seminars offer additional learning and networking opportunities, and provide alternative forums to address specific technological challenges.

The IITC conference website is http://www.ieee.org/conference/iitc. For additional information and inquiries regarding supplier exhibits and seminars, please contact Noel Russell, Sponsorship Chair at Noel.Russell@us.tel.com.

General Co-Chairs of IITC/AMC 2014

Deepak C. Sekar, Rambus Labs
Eric Eisenbraun, SUNY CNSE
Zsolt Tokei, IMEC
Hyun-Chul Sohn, Yonsei University
Noel Russell, TEL

2014 IEEE Symposia on VLSI Technology and Circuits

LATEST DEVELOPMENTS IN MICROELECTRONIC TECHNOLOGY TO BE FEATURED AT THE 2014 SYMPOSIA ON VLSI TECHNOLOGY AND CIRCUITS

JOINT VLSI TECHNOLOGY AND CIRCUITS FOCUS SESSIONS INCLUDE ADVANCED MEMORY TECHNOLOGIES, 3D TSV INTEGRATION, AND THE IMPACT OF SCALING ON ADVANCED DEVICE DESIG…

The 2014 Symposia on VLSI Technology and Circuits will be held at the Hilton Hawaiian Village June 9–12, 2014 (Technology) and June 10–13, 2014 (Circuits). Linked for the past 26 years, the annual Symposia on VLSI Technology and Circuits provide the opportunity for the world's top device technologists, circuit and system designers to engage in an open exchange of leading edge ideas at the world's premier mid-year conference for microelectronic technology. Since 1987, the Symposia on VLSI Technology and Circuits have been held together, alternating each year between sites in the US and Japan, making it possible for attendees to learn about new directions in the development of VLSI technology and circuit design through some of the industry's leading research and development work.

The comprehensive technical programs at the two Symposia are

augmented with short courses, invited speakers and several evening rump sessions. As a new highlight, the Symposia have introduced joint technology and circuit focus sessions in 2012, consisting of invited and contributed papers on topics of mutual interest to attendees.

The **Symposium on VLSI Technology** program will focus on breakthroughs in devices and processes including:

- Memory, logic, RF, analog, mixed-signal, I/O, high-voltage, imaging, and MEMS
- Advanced gate stacks, channels, junctions, contacts and interconnects
- Heterogeneous integration of non-Si materials/substrates on Si substrates
- Advanced lithography and high-density VLSI patterning technologies
- Beyond-CMOS functional devices with a path for VLSI implementation
- Packaging technologies, through-silicon-vias (TSVs) and 3D-system integration
- Advanced materials, device analysis, and modeling
- Theoretical understanding, operation fundamentals and reliability issues related to the above devices
- VLSI manufacturing concepts and technologies

The **Symposium on VLSI Circuits** program will showcase innovations and advances in the following areas:

- Digital circuits and processor techniques, including circuits and techniques for standalone and embedded processors
- Memory circuits, architectures, and interfaces for volatile and non-volatile memories, including emerging memories
- Clock generation and distribution for high-frequency digital and mixed-signal applications
- Analog and mixed-signal circuits, including data converters, sensor interface circuits, and amplifiers
- Wireline receivers and transmitters, including circuits for inter-chip and long-reach applications
- Wireless receivers and transmitters, including circuits for WAN, LAN, PAN, BAN, and inter-chip applications
- Power management circuits, including battery management circuits, voltage regulators, energy harvesting circuits, and circuits for renewable energy applications
- Application-oriented circuits and VLSI systems, including biomedical applications, and including SoC and SiP architectures and implementations

Joint technology and circuits focus sessions will feature invited and contributed papers highlighting major innovations and advances in materials, processes, devices, integration, reliability and modeling in the following areas of joint interest:

- Design in scaled technologies: Impact of advanced devices, structures, materials and interconnects on digital circuit performance, power, density; device design & process/technology optimization for analog/mixed-signal circuits
- Design enablement: Technology and design co-optimization for improved performance, yield, reliability, ultra-low voltage/power operation, density, and cost
- Memory technologies: Discrete and embedded SRAM, DRAM and NVRAM technology/design co-optimization
- 3D-integration (TSV): 3D-technologies and system co-optimization; power delivery and management; thermal management; inter-chip communications

Best Student Paper Award

Based on the quality of the papers and presentations, an award for best student paper at the Symposia will be chosen, and the recipient will receive a financial prize, travel cost support and a certificate at the opening session of the 2015 Symposium. For a paper to be reviewed for this award, the author must be enrolled as a full-time student at the time of submission, must be the lead author and presenter of the paper, and must indicate on the web submission form that the paper is a student paper.

Paper Submission Deadline

The deadline for paper submissions to both conferences is January 27, 2014. Late-news deadline for the Symposium on VLSI Technology is March 27, 2014; there is no late-news submission for the Symposium on VLSI Circuits. Complete details for paper submission can be found online at: http://www.vlsisymposium.org/authors/.

Hilton Hawaiian Village Beach Resort Spa

Sponsoring Organizations
The Symposium on VLSI Technology is sponsored by the IEEE Electron Devices Society and the Japan Society of Applied Physics, in cooperation with the IEEE Solid-State Circuits Society.

The Symposium on VLSI Circuits is sponsored by the IEEE Solid-State Circuits Society and the Japan Society of Applied Physics, in cooperation with the Institute of Electronics, Information and Communication Engineers and the IEEE Electron Devices Society.

Further Information, Registration and Official Call for Papers: http://www.vlsisymposium.org.

Chorng-Ping Chang
2014 Publicity Chair
Symposium on VLSI Technology
Applied Materials, Inc.

Gunther Lehmann
2014 Publicity Chair
Symposium on VLSI Circuits
Infineon Technologies AG

2014 IEEE Photovoltaic Specialists Conference (PVSC)

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looking to learn how a multi-junction solar cell works. These courses will provide a focused, rapid education in a range of topics of interest to the PV community.

Technical Program
Above all, the PVSC is renowned for its one-of-a-kind technical program, where the world's leading voices in PV present their latest findings and offer forward-looking insights on the future of the industry. For the 40th meeting, we are expecting over 1,000 submissions, which will bring you an unparalleled educational experience across 12 topical areas:

Area 1. Fundamentals and New Concepts for Future Technologies
Area 2. Thin Film Polycrystalline Photovoltaics
Area 3. III-V and Concentrator Technologies
Area 4. Crystalline Silicon Photovoltaics
Area 5. Thin Film Silicon Based PV Technologies
Area 6. Organic Photovoltaics
Area 7. Space Technologies
Area 8. Characterization Methods
Area 9. PV Modules and Manufacturing
Area 10. PV Systems and Applications
Area 11. PV Deployment
Area 12. PV Reliability

As you can see, our technology focus spans from the basic technologies through system development and characterization, to deployment. Area 7 is one to highlight, as the PVSC is the only PV technology conference that maintains a focus of space technologies, which is the birthplace of PV for electric energy generation and continues as the incubator for high efficiency technologies. Areas 9 through 12 form our PV system development and deployment thrust in which we track the transition of PV technologies from development to use in the field and analyze the on-station performance. With this line up of topical areas, the technology that you are developing or interested in learning about (or both!) will be sure to find a home at the PVSC.

The PVSC Exhibit hall will be providing an action-packed floorshow with an extensive list of companies eager to interface with the PV specialists at the conference. The theme for our exhibits is tools for the PV specialist. Being the premier technical PV conference, the exhibiters will be those serving the needs of the PV specialist, displaying the latest in solar simulator capability, electrical material characterization, semiconductor growth tools, and many more. Our exhibit hall will resemble a toy store for the child in all of our PV specialists.

Our student program is worth noting, as the PVSC endeavors to foster as much student participation as possible. We facilitate access to the conference with a reduced student registration rate, and the graduate student assistant program, and we strive to enhance the student's conference experience with events like our student mixer and the best student paper award. We also maintain our PV Jobs portal, which is of keen interest to our students and to our community as a whole.

So, as you can see, the IEEE PVSC 40 is shaping up to be our most exciting conference yet, so be on the look-out for our First Call for Papers and mark your calendar for the abstract submission deadline of February 10, 2014 and the conference date of June 8–13, 2014.

Rebekah Feist
2014 PVSC Publicity Chair
Dow Chemical
Saginaw, MI, USA

Society News

EDS Incoming President's Message

Albert Wang
EDS President
2014–2015

Dear Fellow EDS Friends,

I am honored to write to you as the new EDS President. For about twenty years, EDS has been helping me in my career training, development and transition. Now, it is the time for me to take the leading role as the dedicated, enthusiastic and chief volunteer, my definition for the EDS President, to promote the EDS vision, execute the EDS mission, and serve the EDS community.

With about 10,000 members and about 174 chapters around the globe, EDS has been contributing critically to advancing the human society since 1952 by continuously developing and delivering various "electron devices," which are the foundation elements of modern information technologies. Looking forward, EDS will continue to play the key role to benefit the human society.

I believe that EDS must be more flexible and adaptive to the rapid-changing field with quick and early involvement in emerging technologies. I believe that EDS must continue its globalization efforts by penetrating the emerging regions aggressively while holding our existing grounds. I believe that EDS must continuously attract volunteers by member involvement and recognition. I believe that EDS must develop and deliver meaningful products to address its member needs in career enhancement and transition. As the EDS President, I promise to work diligently to promote the EDS values and serve the EDS community.

I would like to express my sincerest appreciation to my predecessor, Paul Yu, and the retiring ExCom team for their hard work during the past two years.

Looking ahead, there are opportunities and challenges for EDS. As the chief volunteer, I will work closely with all of you to make sure that EDS will become better and contribute more to the well-being of humanity.

Albert Wang
EDS President
University of California,
Riverside, CA, USA

EDS Outgoing President's Message

Paul Yu
EDS President
2012–2013

Dear All,

It's been said that the days are long and the years are short.

Looking back at my tenure as EDS president, I remember many such days (and nights) travelling around the world, working late into the night with our dedicated volunteers and staff, to advance the vision and mission of EDS. Yet somehow it's hard to fathom that my time as President of this wonderful society has, in seems like the blink of eye, come to pass.

In my previous message I spoke of our major accomplishments and new initiatives now underway, including our General Election pilot and the establishment of the EDS Mission Fund. But in this message, I want to focus on something more important than the work of EDS… and that's the volunteers and members of EDS.

When I think of the amazing people I have worked with in these past two years, I am humbled and honored to have served as your President. I want to take a moment to thank you all for this opportunity and for allowing me to share in the stewardship of the Electron Devices Society. The list of people to thank is far too long to mention everyone as there are literally hundreds of volunteers without whom the successes of my presidency would not be possible. That being said, I do owe a special debt of gratitude to the following EDS volunteers:

The EDS Executive Committee—President Elect, Albert Z.H. Wang; Sr. Past President, Cor L. Claeys; Jr. Past President, Renuka P. Jindal; Secretary, Fernando Guarin; Treasurer, Ravi M. Todi; Vice President of Awards, Marvin H. White; Vice President of Educational Activities, Meyya Meyyappan; Vice President of Meetings, Bin Zhao; Vice President of Membership, Jamal Deen; Vice President of Publications, Samar K. Saha; Vice President of Regions & Chapters, Xing Zhou; and Vice President of Technical Activities, Joachim N. Burghartz.

Elected Members-at Large—Arturo Escobosa, Juin J. Liou, Mikael Ostling, M.K. Radhakrishnan, Zeynep

Celik-Butler, Mansun J. Chan, Steve S. Chung, Simon Deleonibus, Tian-Ling Ren, Enrico Sangiorgi, Daniel Mauricio Camacho Montejo, Subramanian Iyer, Arokia Nathan, Michael Shur, Douglas P. Verret.

These people are the true leaders of EDS, and it is their guidance, insight, intelligence, and unwavering dedication that has made, and will continue to make, EDS the world's premier society devoted to the advancement of device engineering.

I was also blessed to have had the full support of the EDS staff led by Executive Director Chris Jannuzzi, whose dedication and resourcefulness have touched upon the members and the volunteers. In particular, I like to thank Laura Riello, Jean Bae, Kellie Gilbert, Marlene James, Joyce Lombardini, Jo Ann Marsh, Mariola Piatkiewicz, and Rosemary Schreiber for their continuous support of the EDS activities and the committees.

Serving as President is a great honor I will forever cherish and I want to thank each and every one of you for making this amazing experience possible. I offer you my sincerest thanks and gratitude.

Paul Yu
EDS President, 2012–2013
University of California at San Diego
San Diego, CA, USA

Message from the EDS Newsletter Editor-in-Chief

M.K. Radhakrishnan
Editor-in Chief,
EDS Newsletter

Dear Members,

In my first message to you all, I mentioned that one of the initial priorities of our Newsletter Editorial team is to bring the news from the Society as fast as possible to the members. To that end, the latest information from the BoG meeting held on 08 December 2013 is included which comprises the list of newly elected BoG members and officers as well as the message from Albert Wang as he takes charge as our Society President.

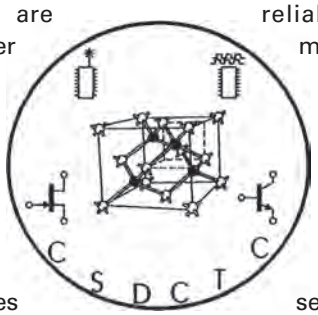
Our aim is to make the Newsletter a more useful avenue to the members for networking, professional development, and knowing each other. As such, we are planning to include appropriate columns to cover latest technological development in the field, as well as social activities of the members and chapters, in future issues. The significance of all these has to be viewed by EDS members in our global family of professionals spanning six continents and through more than 170 chapters worldwide.

As members of a global family, we need to further improve our communication, provide visibility to our activities and to know our sufferings and happiness as professionals. In order to make all these happen, on behalf of the Editorial team and staff, I request your feedback and opinion on how to make EDS newsletter a better medium. Please send your feedback mails to: edsnewsletter@ieee.org

M.K. Radhakrishnan
Editor-in Chief, EDS Newsletter
NanoRel, Bangalore, India
e-mail: radhakrishnan@ieee.org

EDS Compound Semiconductor Devices and Circuits Technical Committee Report

Research on compound semiconductor (CS) electronics is showing continuous advances in traditional areas and new fields. Microwave and mm-wave applications are benefiting from further developments in well-established technologies (e.g. III-V HEMTs and HBTs), while research in III-V MOSFETs and FINFETs as a possible alternative to Si-based digital devices has reached interesting milestones. Progress in widegap (SiC and GaN) electronics continues and a steady improvement is seen in the related reliability issues. Further major advancements are found for the application of III-N concepts to power electronics for fast switching in energy conversion. At the same time, the quest for graphene-like 2D semiconductors has also found an interesting CS line in the 2D transition metal chalcogenides.



The main driver of the development of III-V MOSFETs lies in the superior electron transport properties of III-V materials with respect to Si, enabling an attractive route to downscaling at sub 10 nm nodes. Different architectures have been considered for aggressively scaled III-V devices; examples are the FINFET, the Nanowire FET (also called Gate All Around, GAA FET), the Extremely Thin Body Quantum Well

(ETB-QW) FET. ETB-QW FETs exploit a metal gate, high-κ insulator, and an InGaAs/InAs/InGaAs composite channel. ETB-QW InAs MOSFETs with improved electrostatics, 50 nm gate length and subthreshold swing (SS) in excess of 100 mV/dec, DIBL of 73 mV/V, off-state current of 0.5 nA/μm and maximum g_m > 1.5 mS/μm at V_{DS} = 0.5 V were presented in 2012 at IEDM by researchers from SEMATECH, Globalfoundries, MIT, UT-Austin, CNSE, TEL and HKUST, see the IEDM 2012 Proc., p.32.3.1. Researchers from Purdue and Harvard Universities presented (see IEDM 2012 Proc., p.27.6.1) 20 nm–80 nm channel length strained InGaAs GAA nanowire FETs with record high on-state and off-state performance by equivalent oxide thickness (EOT; the insulator exploits Al_2O_3 and $LaAlO_3$ layers) and nanowire width scaling down to 1.2 nm and 20 nm, respectively; performances included a SS = 63 mV/dec, DIBL as low as 7 mV/V, ION = 0.63 mA/μm and g_m = 1.74 mS/μm at V_{DS} = 0.5 V, demonstrating the promise of InGaAs GAA FETs for 10 nm and beyond high-speed low-power digital applications. The same research groups (see the IEDM 2012 Proc., p.23.7.1) proposed a vertically stacked nanowire array GAA InGaAs FET (imaginatively called 4D GAA FETs) achieving a 4x increase of the driving current and g_m versus the 3D (non-stacked array) version. The device exhibits a record high I_{ON} = 9 mA/μm and g_m = 6.2 mS/μm. The III-V 4D transistor structure appears promising also in the RF and microwave analog field.

During the last few years, the development of widegap semiconductor devices, in particular GaN-based, has undergone a steady progress. For an overview of recent advances the reader can refer to the October 2013 (vol.60, no.10) Special Issue of the IEEE ED Trans. on GaN electronics. As mentioned, developments have concerned not only the traditional RF and microwave power, but also power switching applications with lower-cost GaN on Si devices.

The progress of RF, microwave and millimeter wave GaN HEMTs has led to cutoff frequencies exceeding 450 GHz and oscillation frequencies close to 600 GHz in devices with optimized asymmetric layout and nanometer-scale gate lengths, see the paper from HRL Laboratories (IEEE ED Trans., vol.60, no.10, p.2982). TrQuint reports both E-mode and D-mode InAlN/AlN/GaN HEMTs with gate lengths in the 30 to 50 nm range with frequency performance well in excess of 200 GHz and a noise figure of 0.25 dB at 10 GHz, see IEEE ED Trans., vol.60, no.10, p.3099. Also in high-frequency applications, properly optimized AlGaN/GaN HEMTs grown on Si substrates have shown a power density of 1.5 W/mm at 40 GHz, see IEEE ED Trans., vol.60, no.10, p.3105.

Concerning power switching applications, wide-bandgap semiconductors such as SiC and GaN are witnessing rapid increase in R&D as well as capital investment for next-generation power conversion & management systems with higher efficiency. With SiC MOSFETs being exploited in vertical structures for its high current density, the development of GaN-based power transistors focuses on the lateral heterojunctions (e.g. AlGaN/GaN) for the material maturity. Major efforts being made to tackle key technology challenges include: i) finding the suitable gate dielectrics with a low interface trap density for improved threshold voltage stability; ii) optimizing buffer structures for high breakdown and low dynamic ON-resistance on large-area silicon substrates; and iii) optimizing passivation techniques and field-plate structures for improved device reliability/stability. We are also witnessing a significant increase in product announcements of GaN power devices covering a wide range of voltage rating (30 V ~ 600 V) during the last year.

Significant advances have also been made in the development of GaN-based MOSFETs. With respect to SiC, the GaN MOSFET has higher mobility for higher speed application and lower power consumption during turn-on. Compared with AlGaN/GaN HEMTs, the GaN MOSFET has the advantages of positive threshold voltage, lower leakage current and superior reliability for power electronics. To lower the cost, the GaN should be grown on Si substrate that has a large wafer size up to 12 inch. Nevertheless, the high tensile strain of GaN can create crack in the Si substrate. One solution is to add the compressive strained AlSiC layer before the epitaxial AlN buffer layer and the GaN/AlGaN layer (IEEE EDL 34, p. 975, Aug. 2013). Besides, good device performance of normally-off, gate-recessed GaN MOSFET was reached with a 600 V breakdown voltage, in addition to the crack-free surface. This technology may lead to grow GaN/AlGaN on large size Si wafers.

Recently, the new area of graphene-like 2D compound semiconductors opened up with the family of transition metal dichalcogenides. Similar to graphite, these can be exfoliated into single mono- or multilayers and deposed onto Si substrates. Molybdenum disulfide (MoS_2) probably is the most important material nowadays; although its mobility is of the order of 100 cm^2/V.s only, MoS_2 mono- and multilayers, contrarily to graphene, have a bandgap, direct (2 eV) and indirect (1.8 eV), respectively. This allows the fabrication of thin-film transistors with excellent switch-off with E-mode D-mode operation, but also of sensors and photodetectors, as potential substitutes of Si in conventional electronics and of organic and amorphous Si in systems and display applications. The first MoS_2 TFT was presented by

Kis et al. of EPFL in 2011 (see Nature Nanotech., vol. 6, no. 3, pp. 147–150, 2011) but many research groups are engaged in the development of this technology, see e.g. the multilayer MoS_2 transistor presented at IEDM in 2012 (pp. 5.5.1–5.5.4) and the bilayer MoS_2 integrated circuits (implementing logical functions and ring oscillators) in Nano Letters, 2012, 12 (9), pp. 4674–4680.

The 2013 EDS CSDC Committee member list can be found at: http://eds.ieee.org/technical-committees/eds-compound-semiconductor-devices-and-circuits-technical-committee.html. Some of the CSDC committee members have been guest editors of the October 2013 ED Trans. SI on GaN electron devices and in the chapter *RF and microwave semiconductor technologies* of the EDS anniversary book *Guide to state-of-the-art electron devices*, J. Burghartz, ed., Wiley-IEEE, 2013. Among future activities the EDS CSDC Committee would continue proposing special issues in the EDS periodicals focused on recent developments in the area.

Giovanni Ghione
EDS CSDC
Technical Committee Chair
Politecnico di Torino, Italy

Kevin Chen
Hong Kong University of Science & Technology

Albert Chin
National Chiao Tung University, Taiwan

Ruediger Quay
Fraunhofer Institute, Freiburg, Germany

Call for Nominations—IEEE Fellow Class of 2015

IEEE Fellow is a distinction reserved for select IEEE members. The honor is conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest.

If you know of an IEEE colleague who is a Senior Member or Life Senior Member in good standing, has completed five years of service in any grade of IEEE Membership and who has made an outstanding contribution to the electronic or electrical engineering profession in any of the IEEE fields of interest, you can nominate this person in one of four categories: Application Engineer/Practitioner, Educator, Research Engineer/Scientist or Technical Leader. Nominations for the Fellow Class of 2015 are now being accepted.

To learn more about the Fellow program and the application process, visit the Fellow Web Site at http://www.ieee.org/fellows. The deadline for nominations is March 1, 2014.

Congratulations to the 21 EDS Members Recently Elected to IEEE Senior Member Grade!

Khaled Addoweesh
Kerem Akarvardar
Mohammad Bukhari
Edward Cartier
John Cetnar
YoungHo Cho
Robert Gateru
Bahram Ghodsian
Sanjay Ghosh
Zachary Griffith
Emanuel Istrate
Karol Kalna
Martin Kerber
Chien-Chung Lin
James Masi
Tapas Pal
Pierpaolo Palestri
Thomas Szkopek
Miguel Urteaga
Michael Wright
Gregary Zweigle

* Individual designated EDS as nominating entity.

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status.

Please remember to designate the Electron Devices Society as your nominating entity!

For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application: https://www.ieee.org/membership_services/membership/senior/application/index.html

You will need to Sign-in with your IEEE account.

Announcement of the 2013 EDS Ph.D. Student Fellowship Winners

Agis Iliadis
EDS Student Fellowship Chair

The Electron Devices Society Ph.D. Student Fellowship Program was designed to promote, recognize, and support Ph.D. level study and research within the Electron Devices Society's field of interest: The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

The Society is concerned with research, development, design and manufacture related to materials, processing, technology, and applications of such devices, and scientific, technical, educational and other activities that contribute to the advancement of this field.

EDS proudly announces three EDS Ph.D. Student Fellowship winners for 2013. Brief biographies of the recipients appear below. Detailed articles about each Ph.D. Student Fellowship winner and their work will appear in forthcoming issues of the EDS Newsletter.

Tarek Zaki (S'07) received the B.Sc. degree (with highest honors) in information engineering and technology from the German University in Cairo (GUC), Egypt, in 2009, and the M.Sc. degree (with distinction) in micro- and optoelectronics from the University of Stuttgart, Germany, in 2010. He joined the Institute for Microelectronics Stuttgart (IMS CHIPS) and the Institute for Nano- and Microelectronic Systems (INES), Germany, as a researcher in 2010 and 2011, respectively, where he is currently working towards the Ph.D. degree under the supervision of Prof. Dr.-Ing. Joachim N. Burghartz. His research focuses on the development of world's fastest low-voltage thin-film transistors and mixed-signal circuits based on organic semiconductors. He authored/co-authored more than 15 peer-reviewed, papers at top publication venues. He is a member of the IEEE EDS and SSCS.

Hong-Yu (Henry) Chen received his B.S. degree from National Tsing Hua University (NTHU), Hsinchu, Taiwan, in 2007 and his M.S. degree from Stanford University, CA, in 2011, both in electrical engineering. He is currently pursuing his Ph.D. degree at Stanford University under the supervision of Prof. H.-S. Philip Wong.

Henry's research interests at Stanford include (1) processing technology and the characterization of emerging resistive switching memory; (2) carbon nanotubes material synthesis, device characterization, and circuit integration. To date, he has authored/coauthored 40+ technical papers, including 1 ISSCC, 4 VLSI, and 7 IEDM papers. His papers have been cited more than 150 times since 2010 with H-index 7.

Henry held summer internship positions at Applied Materials Inc., IMEC, and SanDisk Inc. in 2011, 2012, and 2013 respectively. He is the recipient of several awards, including the Intel Fellowship 2013–2014, Taiwanese Government scholarships to study abroad (GSSA) 2012–2014, the IEEE Electron Devices Society Ph.D. Student Fellowship 2013, and the Best Student Paper Award of the 2011 VLSI Technology Symposium.

HeTian received the B.S. degrees from HeFei University of Technology, China in 2010. Since 2010, he has worked at the Institute of Microelectronics, Tsinghua University, China, as a Ph.D. student. He is currently a young team leader investigating novel flexible graphene-based devices. He has already published 12 first-authored papers, which appeared in top venues such as Nano Letters, ACS Nano, Scientific Reports, Nanoscale, Applied Physics Letters, etc. He has also reported his research outcomes at top conferences such as the IEEE IEDM and MEMS. Mr. Tian has been an active student volunteer for EDS activities and serves as Vice Chair of the IEEE EDS Tsinghua University Student Chapter.

Agis Iliadis
EDS Student Fellowship Chair
University of Maryland
College Park, MD, USA

2014 PhD Student Fellowship

Description: One year fellowships awarded to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest. The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

It is expected that three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Middle East/Africa, and Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$5,000 to the student and if necessary funds are also available to assist in covering travel and accommodation costs for each recipient to attend the EDS Administrative Committee meeting for presentation of the award plaque. The EDS Newsletter will feature articles about the EDS PhD Fellows and their work over the course of the next year.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be pursuing a doctorate degree within the EDS field of interest on a full-time basis; and continue his/her studies at the current institution with the same faculty advisor for twelve months after receipt of award. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electron devices and a proven history of academic excellence.

May 15, 2014
Submission Deadline

Nomination Package

- Nomination letter from an EDS member
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date
- One-page biographical sketch of the student (including student's mailing address and email address)
- One copy of the student's under-graduate and graduate transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.
- Two letters of recommendation from individuals familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2014**
- Recipients will be notified by July 15
- Monetary awards will be given by August 15
- Formal award presentation will take place at the EDS Board of Governors Meeting in December

EDS is now accepting nomination package submissions via e-mail, fax and mail!

Email: edsfellowship@ieee.org
Fax: +1-732-235-1626

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-phd-student-fellowship-program.html

Announcement of the 2013 EDS Masters Student Fellowship Winners

Agis Iliadis
EDS Student
Fellowship Chair

The Electron Devices Society Masters Student Fellowship Program was designed to promote, recognize, and support Masters level study and research within the Electron Devices Society's field of interest. The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

The Society is concerned with research, development, design and manufacture related to materials, processing, technology, and applications of such devices, and scientific, technical, educational and other activities that contribute to the advancement of this field.

EDS proudly announces three winners of the 2013 EDS Masters Student Fellowship. Brief biographies of the recipients appear below. Detailed articles about each Masters Student Fellowship winner and their work will appear in forthcoming issues of the EDS Newsletter.

Enes Battal received the B.S. degree in Electrical and Electronics Engineering from Bilkent University, Ankara, Turkey. He is currently pursuing his Master's Degree under supervision of Asst. Prof. Ali Kemal Okyay in the same department. His undergraduate research activities focused on utilizing surface plasmons to achieve functional structures and enhanced optical absorption. He is currently working on development and characterization of actively tunable optical materials and their use in the realization of novel reconfigurable optical nanodevices. He is also interested in development of material alternatives to metals to be used in plasmonics. He has authored or co-authored 5 journal papers and more than 10 conference papers.

Zhongyu Li is a graduate student at the University of Electronic Science and Technology of China. His research interests mainly concern novel radar imaging. Till now, he has published five papers on several international journals and conferences, and also published six papers as the second author in *IEEE Transactions on Geoscience and Remote Sensing, IEEE Transactions on Aerospace and Electronic Systems, etc.* He has successfully applied six Chinese patents for invention.

During his undergraduate study, Zhongyu was awarded with the National Scholarship in 2009 and 2010. In June 2012, he was awarded Excellent Undergraduate Student of Sichuan province.

Yang Lu received the B.S degree in Microelectronics from Peking University, Beijing, China, in 2012. He is currently working toward the M.S. degree at the University of Pennsylvania, Philadelphia, Pennsylvania. Since 2011, Yang Lu has been working on Resistive Random Access Memory (RRAM) in various material systems, including metal oxide based, filamentary RRAM and silicon based, nanometallic RRAM. He and his colleagues investigated switching mechanisms and degradation behaviors in RRAM and developed a simplified model for RESET process. He has published his work in *IEEE Electron Device Letters, IEDM* 2011, IRPS 2012, NVMTS 2013, etc.

Agis Iliadis
EDS Student
Fellowship Chair
University of Maryland
College Park, MD, USA

EDS-ETC

Engineers Demonstrating Science:
an Engineer Teacher Connection

Project Electron Joins Local Science Fair

In 2012, Project Electron joined the Science Circuit of Planaltina, becoming a partner in initiatives promoted by the Secretary of Education of the Federal District of Brazil.

The project was presented to an audience composed mainly of students from primary and secondary public schools. Tests were performed using donated Elenco Snap Circuits® kits that included FM radio and human transistor experiments.

Several *teachers expressed interest in the project and requested information for possible implementation in their schools.* It was very enriching to attend this event because it was an opportunity to demonstrate this program to more communities and educators.

Rafael Amral Shayani
IEEE Centro-Norte Brasil
Section Chair

2014 Masters Student Fellowship

Description: One-year fellowships awarded to promote, recognize, and support graduate Masters level study and research within the Electron Devices Society's field of interest: all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

Three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Mid-East/Africa, Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$2,000 and a plaque to the student, to be presented by the Dean or Department head of the student's enrolled graduate program.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be accepted into a graduate program or within the first year of study in a graduate program in an EDS field of interest on a full-time basis; and continue his/her studies at a graduate education institution. Nominator must be an IEEE EDS member and preferably be serving as the candidate's mentor or faculty advisor. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform research in the fields of electron devices and proven history of academic excellence in engineering and/or physics as well as involved in undergraduate research and/or supervised project.

May 15, 2014
Submission Deadline

Nomination Package

- Nomination letter from an EDS member who served as candidate's mentor or faculty advisor.
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date. This can include undergraduate, graduate and summer internship research work.
- One-page biographical sketch of the student (including mailing address and e-mail address)
- One copy of the student's transcripts/grades
- One letter of recommendation from an individual familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2014**
- Recipients will be notified by July 15
- Monetary awards will be presented by the Dean or Department Chair of the recipient's graduate program at the beginning of the next academic term.

EDS is now accepting nomination package submissions via e-mail, fax and mail!

Email: edsfellowship@ieee.org
Fax: +1 732-235-1626

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-masters-student-fellowship-program.html

EDS Distinguished Lecturer And Mini-Colloquia Programs

The EDS Distinguished Lecturer (DL) Program exists for the purpose of providing EDS Chapters with a list of quality lecturers who can potentially give talks at local chapter meetings.

To arrange for a lecture, EDS chapters should visit the EDS website to view the listing of EDS DLs and contact the EDS DL directly. A general guideline for the visit, but not the absolute rule, is that the lecturer should be able to include the meeting site with an already planned travel schedule at a small incremental cost to the travel plan. Although the concept of the program is to have the lecturers minimize travel costs by combining their visits with planned business trips, EDS will help subsidize lecturer travel in cases where few/no lecturers will be visiting an area and/or a chapter cannot pay for all the expenses for a lecturer trip.

EDS is also encouraging Distinguished Lecturer clusters/mini-colloquia (MQ) to remote areas. This concept generally involves the sending of about 2 or more DLs to travel to a region/chapter and present the latest developments in a particular field. The chapters/regions would be responsible for handling all the arrangements of the event and only minimal financial support would be required of EDS and could be covered by the MQ Program budget upon request.

For more information on the DL or MQ Programs, please visit the EDS website or contact Laura Riello of the EDS Executive Office.

QuestEDS

Samar Saha
EDS Vice-President of Publications

Interested in knowing why it's not possible to measure the built-in voltage of a PN junction using a voltmeter? Do you need to understand the best way to derive an expression for the average thermal velocity of an electron? Or are you curious about what quantum dots and wires are? The answers to these questions and more are available through the QuestEDS Question and Answer page.

To ask a question not already addressed on the Q&A page, visit www.ieee.org/go/questeds. Technical experts answering the questions posed represent academic, government, and industry sectors.

Questions are grouped into nine technical categories and two general ones. Technical categories cover subject areas like semiconductor and device physics, process technology, device characterization, technology CAD, compact modeling, VLSI interconnects, photovoltaics, and quantum electronics. Subject areas addressed are anticipated to expand in the future. Two other categories address questions pertaining to educational activities and general inquiries about society membership. Within a two week time frame from when the question is asked, an answer is posted online. Incoming questions are handled by an editor-in-chief who ensures that they fall within the technical scope of EDS and that they are adequately answered.

Organic Semiconductor Devices

Question 060–13
Considering that an organic semiconductor, such as "Tips-pentacene", was spin-coated on top of an aluminum sheet, sintered and subjected to a final 3rd layer of gold (applied using a square shadow mask), what would be an appropriate set of formulas that would predict the current dynamics as a function of the voltage and geometry of the layers in this Schottky device?

If the same experiment were performed, but this time applying the tips-pentacene by drop-cast, how should expectedly vary the results? Does the rugosity of the layers affect the performance of the device? Why should one consider the rugosity relevant?

Photovoltaics

Question 061–13
In a solar cell, we want to collect the photo-generated electrons and holes in separate terminals and so we want them not to recombine before collection. In a multi-junction solar cell, current flows from one pn junction to another through tunnel junction, where electron makes a tunneling jump from conduction band to valence band and with so many holes in the valance band, the jumping electron should recombine with hole. So, how can the photo-generated electrons and holes make it to the opposite electrode without recombination in a multi-junction solar cell?

For the answer to this recent submission, visit http://eds.ieee.org/member-sign-in-form.html?notauth=1. Your IEEE login is required to view the answer page. After authentication you will be redirected to the answer page, where you can select the appropriate topic link.

Samar Saha
EDS Vice-President of Publications
Ultrasolar Technology
Santa Clara, CA, USA

2011-2012 EDS Region 9 Outstanding Student Paper Award

The Electron Devices Society confers its prestigious Region 9 Outstanding Student Paper Award to the best Region 9 student paper published in an internationally recognized IEEE sponsored journal or conference in the field of electron devices related topics. The winning paper is entitled, *"Surface-Potential-Based Drain Current Analytical Model for Triple-Gate Junctionless Nanowire Transistors."* This paper was published in the *IEEE Transactions on Electron Devices*, and was authored by Renan Trevisoli Doria, Rodrigo Trevisoli Doria, Michelly de Souza, Samaresh Das, Isabelle Ferain, and Marcelo Antonio Pavanello. The award was presented at SBMicro 2013, which was held September 3–6, 2013, in Curitiba, Brazil. The Award consists of a certificate and reimbursement of up to US $1,500 to cover one author's travel and accommodations to attend the conference. On behalf of the Electron Devices Society, I would like to congratulate Renan Trevisoli Doria and the remaining authors for this achievement. Brief biographies of all the authors of the paper are given below.

Renan Trevisoli Doria received the electrical Engineering degree from Centro Universitário da FEI, Brazil, in 2007, receiving the awards "Prêmio CREA-SP de Formação Profissional" and "Instituto de Engenharia" given for the best student among the 7 modalities of engineering courses offered at FEI. In 2010 he received the M. Sc. degree in Microelectronics from Centro Universitário da FEI and in April 2013 he received the Ph.D. degree in Microelectronics from University of São Paulo, Brazil. In February 2012, he was with Tyndall National Institute, Cork, Ireland, for electrical characterization of Junctionless Nanowire Transistors. His current interests are electrical characterization, modeling and simulation of SOI multiple gate devices.

Rodrigo Trevisoli Doria received the Electrical Engineering degree and the M. Sc. degree in integrated electronic devices from Centro Universitário da FEI in 2003 and 2007, respectively, and the Ph.D. degree in microelectronics from University of São Paulo, São Paulo, Brazil, in 2010. From November 2009 to March 2010 he was with Tyndall National Institute, University College Cork, Ireland, working with the simulation and electrical characterization of Junctionless Nanowire Transistors (JNTs). He is currently a Postdoc Researcher with Centro Universitário da FEI. He is Member of the Brazilian Microelectronics Society and his current research interests are focused on the simulation, electrical characterization, and modeling of SOI CMOS transistors.

Michelly de Souza (S'05–M'08) received the Electrical Engineering degree from Centro Universitário da FEI in 2002, and the M. Sc. and Ph.D. degrees in 2005 and 2008, respectively, in Microelectronics from University of São Paulo, Brazil. From September 2007 to February 2008 she was with Laboratoire de Microélectronique from Université Catholique de Louvain, Belgium, working in the fabrication and electrical characterization of analog circuits with Silicon-On-Insulator transistors. She is currently Associate Professor at Centro Universitário da FEI, Brazil. She is Member of both the IEEE Electron Devices Society and the IEEE Solid State Circuits and Systems Society, and the Brazilian Microelectronics Society. Her current interests are the electrical characterization, simulation and modeling of SOI devices.

Samaresh Das received the M. Sc. and Ph.D. degree in physics from Indian Institute of Technology Kharagpur, India, in 2005 and 2011, respectively. At Indian Institute of Technology, his research involved on Ge quantum dot based floating gates, light emitters and photo-detectors on silicon substrate. He then worked as a researcher in the Ultimate Silicon Device Group led by Jean-Pierre Colinge at Tyndall National Institute, Ireland. There he worked on the fabrication and characterization of Junctionless Nanowire Field Effect Transistors. In November 2012, he joined the Hitachi Cambridge Laboratory, Cavendish Laboratory. He currently works on silicon based quantum information technology.

Isabelle Ferain received the M.Sc. Degree in Applied Sciences from the University of Mons, Mons, Belgium and the M. Sc. Degree in Electrical Engineering from the Ecole Superieure d'Electricite, Orsay, France, in 2001. She received the Ph.D.

Degree in Electrical Engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 2008. She has authored or co-authored more than 100 peer-reviewed publications and conference contributions on nano-technologies, and has co-authored 4 book chapters on SOI and nanowire field effect transistors. She has been with ON Semiconductor, Oudenaarde, Belgium, with IMEC, Leuven, Belgium, and with Tyndall National Institute, Cork, Ireland where she worked on the fabrication and characterization of SOI Multiple-gate FETs. She is currently a member of the technical staff in Globalfoundries, Malta, New York, working in the Technology Development group.

Marcelo Antonio Pavanello (S'99–M'02–SM'05) received the Electrical Engineering degree from Centro Universitário da FEI in 1993, and the M.Sc. and Ph.D. degrees in Microelectronics from University of São Paulo, São Paulo, Brazil, in 1996 and 2000, respectively. In 2003, he became Professor at Electrical Engineering Department of FEI. From November 2008 to February 2009, he was with the Laboratoire de Microélectronique, Université Catholique de Louvain, Louvain-la-Neuve, Belgium, as Visiting Professor. He has authored or coauthored more than 170 technical papers in journals and conferences, and was an author/editor of six books. Dr. Pavanello is an IEEE EDS Distinguished Lecturer.

Jacobus Swart
EDS Region 9 Outstanding Student Paper Award Chair
State University of Campinas
Brazil

2013 EDS CHAPTER OF THE YEAR AWARD

The EDS Chapter of the Year Award is presented annually to recognize EDS chapters for the quality and quantity of the activities and programs implemented during the prior July–June period.

The EDS BoG recently approved a change in the EDS Chapter of the Year Award to recognize more Chapters region wise. Four awards are being decided for this year, one each for Region 1-7, Region 8, Region 9 and Region 10. The selection criterion remains the same as previous years.

The 2013 EDS Chapter of the Year Award winners are:

Regions 1–7: ED/SSC Baltimore Chapter
Region 8: ED IRE NASU Kharkiv Student Branch Chapter
Region 9: ED/MTT/EMB Brazil Chapter
Region 10: ED Delhi Chapter

Xing Zhou
EDS Vice-President of Regions/Chapters
Nanyang Technological University
Singapore

Fabiano Araujo Soares—Region 9 ED MTT EMB Brazil Chapter Chair

Naresh Das—Regions 1-7 ED SSC Baltimore Chapter Chair

Illia Fedorin—Region 8 ED IRE NASU Kharkiv Student Branch Chapter Chair

Mridula Gupta—Region 10 ED Delhi Chapter Chair

USA, Canada & Latin America (Regions 1-6, 7 & 9)

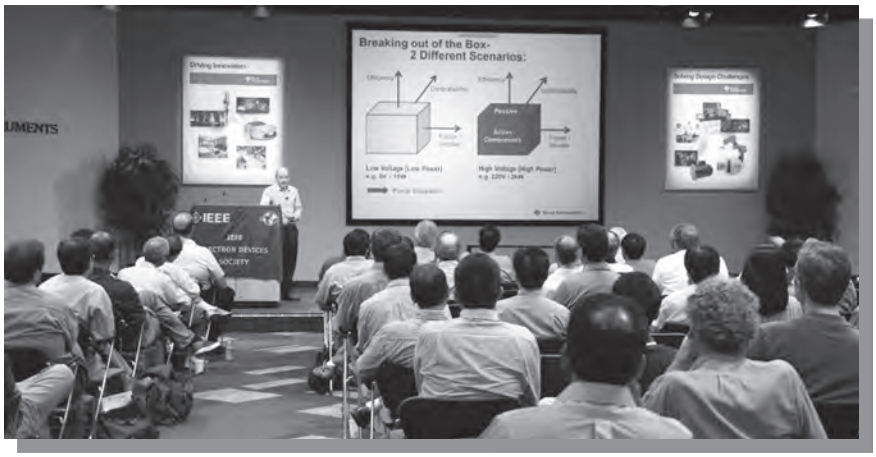
ED Santa Clara Valley

–by Toshishige Yamada

On September 6, 2013, the ED Santa Clara Valley Chapter held its annual Power Electronics Symposium. This year's event titled, "Beyond the Silicon Limit," was located at the TI Auditorium, in Santa Clara, California. The symposium attracted 106 attendees, 76 of whom were IEEE members.

Power electronics is re-emerging as an important and innovative area. This is due to the increasing importance of electricity in our lives, and the need to use it more efficiently. The old paradigm involved large inductors and capacitors, slow silicon devices, and a barrier known as the "silicon limit." The new revolution is fueled not only by improved Si device technology using conductivity and field-modulation, but also by exciting new materials GaN and SiC that have taken devices beyond the silicon limit. Designers are making use of this substantially improved performance to increase efficiency and reduce size. The half-day symposium had presentations from leading contributors in the multidisciplinary field of power electronics. Topics included Si, SiC and GaN device technology, the bottlenecks to power switching, and power electronics applications. The symposium was of significant interest to both device and circuit engineers, students and experts, who wished to develop a broader perspective and increase their depth and breadth of knowledge.

Attendees were privileged to hear the following speakers:



Presentation by Dave Anderson, Texas Instruments

Sandeep Bahl, EDS Chapter Vice-Chair (left) and Don Disney, Avogy (right)

- Deva Pattanayak (Senior Director at Vishay Siliconix)— *"High Voltage Silicon Power Devices below the Silicon Limit"*
- Alex Lidow (CEO of EPC)— *"GaN —the End of the Road for Si"*
- Dave Anderson (Chief Technologist and General Manager of Texas Instruments Kilby Labs Silicon Valley)— *"Power Electronics Applications"*
- Johan Strydom (Head of Applications Engineering at EPC)— *"Barriers to High-speed Switching in Power Devices"*
- Don Disney (Sr. Director of Technology and Product Development at Avogy)— *"Vertical Power Devices in Bulk GaN Substrates"*

~Adam Conway, Editor

Toshishige Yamada, EDS SCV Chapter Chair

Europe, Middle East & Africa (Region 8)

Serbian Academy of Science and Arts, Knez Mihailova 35, Belgrade, Serbia

2014 MIEL

–by Ninoslav Stojadinovic

The 29th International Conference on Microelectronics (MIEL 2014) will be held May 11–14, 2014, at the Serbian Academy of Science and Arts, Belgrade, Serbia. The 2014 MIEL Conference will be organized by the IEEE Serbia & Montenegro Section—ED/SSC Chapter, in cooperation with the Faculty of Electronic Engineering, University of Nis, and the Serbian Academy of Science and Arts, with co-sponsorship by the IEEE Electron Devices Society (EDS), the cooperation of the IEEE Solid State Circuits Society (SSCS), and under the auspices of the Serbian Ministry of Education, Science and Technological Development, Academy of Engineering Sciences of Serbia, and Society for ETRAN.

MIEL is one of the most outstanding European conferences providing an international forum for the presentation and discussion of recent developments and future trends in the field of microelectronics. Since 1984, there is an aura of internationalization around the MIEL conferences, providing an opportunity for specialists from both academic and industrial environments worldwide, to meet in an informal and friendly atmosphere and exchange experiences in the theory and practice of microelectronics. MIEL has benefited from EDS technical co-sponsorship since 1995 and in the year 2000 received approval for IEEE EDS co-sponsorship.

The topics to be covered by the technical program of the conference include all important aspects of micro- and nano-electronic devices, circuits and systems, ranging from materials and processes, technologies and devices, device physics and modeling, process and device simulation, circuit design and testing, system design and packaging, and characterization and reliability. Based on the past decade of history, the technical program is expected to consist of about 140 contributed papers by authors from nearly 30 countries, which will be structured into oral and poster sessions. These papers, together with 15 invited papers, will be presented by world leading authorities in the field of micro-and nano-electronics, and will form a solid foundation for the conference. The associated Mini-Colloquia on nano-technologies and nano-devices will round off the MIEL technical program.

The invited lectures are:

- "2-D Nanocrystals for Next-Generation Green Electronics" (K. Banerjee, University of California, California, USA);
- "On the way to Heterogeneous Nanoelectronics, towards the Zero Power and Zero Variability World" (S. Deleonibus, CEA/LETI, France);
- "Power-Switching Applications Beyond Silicon: The Status and Future Prospects of SiC and GaN Devices" (S. Dimitrijev, Griffith University, Australia);
- "RF MEMS and NEMS Components and Adsorption–Desorption Induced Phase Noise" (Z. Djuric, Serbian Academy of Sciences and Arts, Serbia);
- "Biological circuits for signaling and synchronization in bacterial populations" (P. Hagouel, OPTELEC, Greece);
- "GaN Technology for Power RF: Present State and Future Trends" (P. Igic, Swansea University, UK);
- "Nanoplasmonic Chemical Sensors" (Z. Jaksic, IHTM-CMTM, Serbia);
- "Fabless ASIC Design an Opportunity for Everybody?" (D. Manic, CSEM, Switzerland);
- "Nanotechnology in the Development of Future Nanoelectronic Devices" (M. Meyyappan, NASA, California, USA);
- "Silicon Quantum Dot Devices for Future Electronics" (S. Oda, Tokyo Institute of Technology, Japan);
- "Positrons in Gases and Solids: From Basic Science to Applications" (Z. Petrovic, The Institute of Physics Belgrade, Serbia);
- "High-Resolution Hall Magnetic Sensors" (R. Popovic, EPFL, Switzerland);
- "Modeling Spin-Based Electronic Devices" (S. Selberherr, Technical University Wien, Austria);
- "Lanthana and its Interface with Silicon" (H. Wong, City University of Hong Kong, Hong Kong);
- "A Unified Compact Model for GaN-Based HEMTs" (X. Zhou, Nanyang Technological University, Singapore);

Belgrade is the capital and largest city of Serbia and has a population of about 1.6 million. It is situated in south-eastern Europe, on the Balkan Peninsula, at the confluence of the Sava and Danube Rivers where the Pannonian Plain meets the Balkans. It is one of the oldest cities in Europe and has since ancient times been an important focal point for traffic, an intersection of the roads of Eastern and Western Europe. Belgrade is the capital of Serbian culture, education, science and economy. As a result of its tumultuous history, Belgrade has for centuries been home to many nationalities, with Serbs of the Orthodox Christian religion making up the majority of the population (90%). Belgrade is the seat of the highest scientific and research institutions in all fields. Serbian Academy of Sciences and Arts, one of the organizers of the MIEL 2014 Conference, founded in 1886 as the Serbian Royal Academy, is a leader of the Serbian scientific society in many scientific and artistic areas.

For registration and other information, visit the 2014 MIEL Home Page at http://miel.elfak.ni.ac.rs, or contact the MIEL Conference Secretariat, Department of Microelectronics, Faculty of Electronic Engineering, University of Nis, A. Medvedeva 14, 18000 Nis, Serbia; Telephone: +381 18 529 326; Fax: +381 18 588 399; E-mail: miel@elfak.ni.ac.rs.

The MIEL organizers and committee members look forward to seeing you in May 2014.

Participants of the MIXDES Conference, Gdynia, Poland

2013 MIXDES

–by Mariusz Orlikowski

On June 20–22, 2013, in Gdynia, Poland, the annual 20th International Conference "Mixed Design of Integrated Circuits and Systems" —MIXDES, was held. The event was organized by the Technical University of Lodz, the Warsaw University of Technology and Gdynia Maritime University. The conference was co-sponsored by The Institute of Electrical and Electronics Engineers, Poland Section IEEE Election Devices and the Circuits and Systems Societies, and the Polish Academy of Sciences, Committee of Electronics and Telecommunication, Section of Microelectronics and Section of Signals and Electronic Circuits and Systems. The conference was attended by more than 120 scientists from around the world, representing 21 countries.

The comprehensive conference program of 115 presentations consisted of oral, poster and special sessions. This year, the MIXDES 2013 organizing committee had the pleasure to invite six keynote speakers:

- V. Axelrad (SEQUOIA Design Systems, Inc., USA), *Design and Simulation of ESD-Resistant ICs*
- Y.S. Chauhan (Indian Institute of Technology, Kanpur, INDIA), *BSIM Compact MOSFET Models for SPICE Simulation*
- X. Zhou (Nanyang Technological University, SINGAPORE), *Top-down Drift-diffusion versus Bottom-up Quasi-ballistic Formalism in Device Compact Modeling*
- G. Wachutka (Munich University of Technology, GERMANY), *The Art of Modeling and Predictive Simulation in Power Electronics and Microsystems*
- M.H. Fino (University Nova de Lisboa, PORTUGAL), *On the Use of Compact Modeling for RF/Analog Design Automation*
- H. Toshiyoshi (University of Tokyo, JAPAN), *A Mixed-Design Technique for Integrated MEMS Using a Circuit Simulator with HDL*

In addition to the regular program, two special sessions were held:

- *Compact Modeling for More than Moore,* organized by Dr. Daniel Tomaszewski (Institute of Electronic Technology, Poland) and Dr. Władysław Grabiński (GMC Suisse)
- *xTCA for Instrumentation,* organized by Dariusz Makowski, Adam Piotrowski (Lodz University of Technology, Poland), Holger Schlarb (DESY, Germany) and Stefan Simrock (ITER, France)

Based on evaluations of the quality of the papers and presentations, ten of the papers received the Best Paper Award. Additionally Christian Kauth, Marc Pastre and Maher Kayal from EPFL, Switzerland received the IEEE Poland Section ED Society Special Award, presented by the Chapter Chairman.

The 2014 MIXDES Conference will take place in Lviv, Ukraine, as a partner of the 6th International Conference Microwave and Radar Week (MRW-2014). The Preliminary Call for Papers is available at http://www.mixdes.org/downloads/mrw2014.pdf. More information on past and future MIXDES Conferences can be found at http://www.mixdes.org.

ED Poland

–by Henryk M. Przewłocki

An IEEE EDS Distinguished Lecture (DL) was organized on June 21, 2013, at the Institute of Electron Technology (IET) in Warsaw, Poland. Prof. Hiroshi Iwai of the Tokyo Institute of Technology (TIT), and EDS Distinguished Lecturer, presented a talk titled, *"Future of Nano CMOS Technology."* The audience of this event, of approximately 40 people, was composed of IET staff and guests from other Polish institutes and abroad.

Since the group of TIT researchers lead by Prof. Iwai is at the forefront of new developments in nano CMOS technologies, the lecture was a very competent and clear presentation of the DL's opinions on further developments in this area during the coming 10-15 years. The audience enjoyed very much the clear and well-motivated opinions of Dr. Iwai.

~ Zygmunt Ciota, Editor

ED/PHO Dublin

–by Patrick McNally

The Joint chapter of the Dublin Electron Devices and the Ireland Photonics Societies hosted the President-Elect of the Electron Devices Society and Distinguished Lecturer, Professor Albert Wang, on October 3, 2013, at Dublin City University. Professor Wang, of the University of California, Riverside, delivered a seminar entitled "*Concurrent Design of RF Integrated Circuits (ICs) and Electrostatic Discharge (ESD) Protection*." On-chip ESD protection design is a grand challenge in RF IC manufacture and Professor Wang's talk discussed critical aspects in practical designs, including a mixed-mode ESD simulation-design method for RF ESD protection design optimization and prediction, accurate RF ESD design characterization, complex ESD-IC interactions, and ESD+RFIC co-design techniques for whole-chip design optimization.

The talk was attended by more than 30 academic staff and students, as well as other local IEEE members. Using the facilities of Ireland's National Nanotechnology Platform, INSPIRE, the lecture was video-linked live to the Tyndall National Institute in Cork and the University of Limerick. After the seminar, there was also an opportunity to network and meet the speaker.

Dr. Albert Wang at Dublin City University

ED Scotland

–by Jonathan Terry

In its efforts to increase its profile in the technical community, the Scottish chapter of EDS was a technical co-sponsor of the IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2013), which was held in Glasgow last September. The chapter provided the IEEE ED Scotland Best Student Paper Award, which was won by Juan Pablo Duarte of the University of California, Berkeley, for his paper Unified FinFET Compact Model: Modelling Trapezoidal Triple-Gate

Prof. Hiroshi Iwai (5th from left), accompanied by some of the event attendees at the Institute of Electron Technology (IET) in Warsaw, Poland

Professor Albert Wang pictured at Dublin City University with some of the IEEE members who attended his presentation

EDS Distinguished Lecturer, Professor Arokia Nathan of the Department of Engineering at Cambridge University

FinFETs. Other prize winners were Neophytos Neophytou of the Technical University of Vienna who won TCAD Best Paper, and Taichi Misawa of Keio University, Japan who won SISPAD Best Poster.

The chapter has also continued its popular series of lectures, industrial visits and technical workshops. In November, the chapter organized a day of seminars for fifty invited attendees entitled Back to Basics, which was delivered by Agilent Technologies UK. The talks included introductions to Signal and Network Analysis, as well as Measurements of High Power Semiconductors. There was also a product fair of Agilent's toolset at the event. Also in November, Prof. Arokia Nathan, EDS Distinguished Lecturer and the Chair of Photonic Systems and Displays in the Department of Engineering at Cambridge University, gave a well-attended lecture entitled "Amorphous Oxides for Transparent and Flexible Electronics," in which he reviewed the optoelectronic properties of oxide semiconductors, which are known for their optical transparency and high electron mobility even when processed at room temperature, making them a promising candidate for flexible and large area electronics.

Future chapter events include a presentation by Prof. John Robertson, IEEE EDS Distinguished Lecturer and Head of Solid State Electronics and Nanoscale Science Group at Cambridge University. The talk entitled *"Advanced Gate Stacks, High Dielectric Constant Gate Oxides/Metal Gates, Oxides on Semiconductor,"* is scheduled for Wednesday, January 22, 2014, and further details can be found on the chapter's website at http://ieee-ukri.org/eds_scotland_chapter.

~Jonathan Terry, Editor

ED France

–by M. Mouis

Professor Hiroshi Iwai (Tokyo Institute of Technology), IEEE Fellow, Distinguished Lecturer of EDS, shared his vision of the evolution of micro-nano-electronics with an audience of scientists at IMEP-LAHC, in Grenoble Minatec (France) on September 24, 2013. He was invited by Sorin Cristoloveanu, IEEE Fellow, member of the French EDS board. The DL announcement was e-mailed by the chapter chair to all the members of the French EDS chapter and publicized locally.

In his lecture, entitled *"Ultimate CMOS Scaling,"* Professor Iwai enlightened the challenges that the nanoelectronic industry will be facing for the next generations of CMOS circuits. He discussed the ultimate limits, may they be different for high performance and low power applications, and evoked several solutions. The downscaling of the gate stack was one but not the sole example of such a challenge. The lecture illustrated that, while the limits of CMOS downscaling are approaching, no real competitor has yet emerged. Professor Iwai documented the state of the art of alternative device architectures and technologies. His message was that the research efforts need to be intensified in selected domains, despite numerous, difficult and interesting issues are still challenging the development of sub-10 nm nanoscale CMOS.

About 40 researchers, faculties and Ph.D. students attended this lecture, as well as 15 members of the EDS chapter. The lecture allowed different levels of listening, suitable to Ph.D. students but also to the many experts from the Grenoble, Minatec and Crolles area. The audience highly appreciated this excellent lecture and contributed many questions and comments to the debate.

~Jan Vobecky, Editor

Professor Iwai's EDS Distinguished Lecture at IMEP-LAHC (Minatec, Grenoble, France), on September 24, 2013

Asia & Pacific (Region 10)

ED Beijing

–by Jinyan Wang

On September 5, 2013, Prof. Steve S. Chung from the National Chiao Tung University of Taiwan (NCTU), visited the ED Beijing Chapter. With the Chapter's arrangement, he delivered an EDS Distinguished Lecture entitled, *"The Charge Loss Issues in a Two-bit SONOS Flash Memory-Low voltage operating schemes and solutions."* The lecture was held at the Institute of Microelectronics of Chinese Academy of Sciences (IMECAS) and hosted by Prof. Jinyan Wang, the Chapter Chair and Prof. Ming Liu from IMECAS, the vice Chapter Chair. In attendance were more than 30 local professionals and graduate students from the Beijing Chapter.

Prof. Steve gave the recent results on different strategies for designing SONOS-type flash memories with low voltage operation. It is also claimed that a wrapped

gate SONOS enabled better performance for 2-bit per cell operations for achieving excellent data retention. Prof. Steve also explained that the mismatch between electrons and holes could be solved with a good combination of programming/erasing schemes. The new points of his research on SONOS flash memory devices made a big splash and many discussions.

After the lecture, a symposium was held with researchers attending from the Laboratory of Nanofabrication and Novel Device Integration Technology of IMECAS, both sides introduced their recent works and had an effective discussion.

Prof. Steve S. Chung (middle), and Prof. Ming Liu (middle row, 3rd from right) with student members

ED Guangzhou

–by Kong Xuedong

The ED Guangzhou Chapter organized two mini-colloquia at China CEPREI Lab, Guangzhou, on May 30th and July 15th, respectively. The MQ focused on *"Microelectronics Reliability Physics and Qualification."*

Three IEEE EDS Distinguished Lecturers were invited to give talks. Highlight of the seminars included:

- *"Trends in Technology, Reliability and Qualification of Leading Edge CMOS Technologies,"* presented by Dr. Fernando Guarin of IBM Microelectronics Semiconductor Research and Development Center, on May 30th.
- Prof. Juin J.Liou, from University of Central Florida, USA, presented a talk on *"Electrostatic Discharge (ESD) Protection in High-Voltage Si BiCMOS/BCD Technologies,"* on July 15th.
- Prof. Steve S.Chung from National Chiao Tung University, Taiwan, gave a lecture entitiled, *"Guidelines for Developing High-performance and High-reliability strained CMOS Devices,"* on July 15th.

Approximately 90 academic staff from CEPREI and university graduate students attended the mini-colloquia.

Dr. Fernando Guarin (first row, 3rd from right) with some attendees, of the EDS MQ in Guangzhou, May 30, 2013

Attendees at the EDS MQ in Guangzhou, China, July 15, 2013, Prof. Steve S. Chung (first row, 4th from left) and Prof. Juin J. Liou (first row, 5th from left)

ED Peking University

–by Runsheng Wang

The ED Peking University (PKU) Student Chapter held two EDS Distinguished Lectures and one mini-colloquium.

Prof. Steve S. Chung of National Chiao Tung University (on September 6, 2013), and Prof. Mansun Chan from Hong Kong University of Science & Technology (on July 16, 2013), were invited to deliver their lectures, entitled "*Recent Progress on the Carrier Transport of Nanoscale CMOS Device*" and "*Capturing Cellular Communication with a Silicon Integrated Circuit Chip,*" respectively. Both speakers presented their recent studies on various topics, which were very attractive to the attendees.

On July 22, 2013, the ED PKU Chapter successfully held another IEEE EDS Mini-colloquium (MQ) named "*IEEE EDS MQ on Advanced Technology of Micro & Nanoelectronics,*" at the Micro & Nanoelectronics Building of Peking University, Beijing, China. This one-day MQ was supported by the following guest lecturers: Prof. Juin J. Liou (UCF, USA), Prof. Kin Leong Pey (SUTD, Singapore), Prof. Yu (Kevin) Cao (ASU, USA), and Dr. Yangyin Chen (IMEC, Belgium). The event was attended by more than 50 people. Prof. Huang gave the welcome address, followed by a brief introduction to the IEEE Electron Devices Society. The MQ began with Prof. Liou's talk on "*Electrostatic Discharge (ESD) Protection in High-Voltage Si BiCMOS/BCD Technologie,*" followed by Prof. Pey speaking on "*Are Breakdown and Recovery in Ultrathin Gate Dielectrics Similar to Resistive Switching?*" In the afternoon, Prof. Cao presented the "*Hierarchical Exploration of Heterogeneous Memory Design,*" followed by Dr. Chen's talk on "*RRAM in the Past Decade: Technology Evolution and Market Application.*" These lectures covered a broad range of topics on current interests and also produced lively and interactive discussions.

The Peking University chapter held many other events and detailed information can be found on the chapter's website: http://www.ime.pku.edu.cn/soi/edpku.html.

2013 IPFA

–by Alastair Trigg, and Yeow Kheng Lim

The IEEE International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA) is the prominent FA forum in Asia and the flagship

Prof. Steve S. Chung (front row, 6th from the left) pictured with Prof. Ru Huang (front row, 7th from the left), the chapter advisor, and some other members of the Chapter after the DL talk

(front row, from left to right) Prof. Runsheng Wang, Prof. Yimao Cai, Prof. Ru Huang, Prof. Yu (Kevin) Cao, Prof. Juin J. Liou, Prof. Kin Leong Pey, Dr. Yangyin Chen, pictured with some members of the Chapter after the MQ event

X ray 3D CT (Computerised Tomography) image during inspection of C4 solder bumps resembling the storage pots used for fermenting Korean soy sauce. Picture by Chew Su Fang, Xilinx Asia Pacific Pte. Ltd., Singapore – 1st Prize in Art of FA Photo Contest.

Fir Tree Green - Suddenly grown during a FIB cross section by a reaction of Ga-ions with some contamination on the chip surface; the image taken afterwards in a SEM. Picture by Neumann, Infineon Technologies, Munich Germany – 2nd Prize in Art of FA Photo Contest.

conference of the IEEE REL/CPMT/ED Singapore Chapter. The conference was first held in 1987, and with the 2013 occurrence celebrated its 20th anniversary. The 2013 IPFA was held in Suzhou, China, July 15–19, and was jointly organized with the IEEE Nanjing Section ED/SSC Chapter.

The conference began with 2-day tutorials covering various aspects of integrated circuit reliability and failure analysis techniques. During the 3-day symposium, 63 papers were presented orally along with 80 poster presentations. Also, 4 invited papers and the Best Paper exchanges from the 38th International Symposium for Testing and Failure Analysis (ISTFA 2012) and 23rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2012) were presented.

There were 4 keynote papers given by very prominent experts in their fields. Prof. T.P. Ma from Yale University, USA gave the keynote on *"Novel Electrical Characterization Techniques for Reliability Study of Advanced CMOS Gate Dielectrics."* Dr. Shaofeng Xie, from China Electronic Product Reliability and Environmental Testing Research Institute, China presented *"Development and application of prognostics and health management technology."* Dr. Andrew H. Olney from Analog Devices, Inc. USA gave the presentation on *"Eliminating the Top Causes of Customer-Attributable Integrated Circuit Failures."* Dr. John Peng from SMIC China presented *"The Opportunities & Challenges for China's Growing IC Design Houses and Foundries."* IPFA proceedings will be available in *IEEE Xplore*.

An equipment exhibition with more than 30 exhibitors from both local and international companies was held in conjunction with the symposium. FEI Company has remained the Platinum Sponsor since the sponsorship program began 6 years ago. Digit Concept was the Gold Sponsor and Hanwa and Wintech were Silver Sponsors.

The "Art of Failure Analysis" Photo Contest which has become an integral part of IPFA, attracted many FA enthusiasts. Thirty-two FA photos were received for the contest out of which the top 12 voted winners will be published in *IEEE Spectrum*. The best 6 FA pictures won the prizes.

The 21st IPFA conference will be held in Singapore from June 30–July 4, 2014. Details can be found on the conference website: http://ieee-ipfa.org/ .

2013 RSM

–by Mohd Nizar Hamidon and P Susthitha Menon

The IEEE Electron Devices Malaysia Chapter organized the 9th IEEE Regional Symposium on Micro and Nanoelectronics (IEEE-RSM2013) at the Holiday Villa Beach Resort, Langkawi, Kedah, Malaysia, September 25–27, 2013. The conference was locally co-organized by Universiti Putra Malaysia (UPM) as well as Universiti Malaysia Perlis (UniMAP). The ED Malaysia Chapter organizes this event every two years, as a forum for researchers from Malaysia and other Asian countries to share their research findings. RSM 2013 had 106 contributed papers for oral presentation in different parallel sessions of Circuits, VLSI & Microwave, Materials & Process, Nanotechnology, MEMS & Microsensors, Materials & Devices and Photonics. There were more than 130 attendees, representing five countries in Asia. The opening ceremony, as well as the gala dinner, was held on day one, officiated by Dr. Burhanuddin Yeop Majlis, founding Chair of the RSM and Director of the Institute of Microengineering and Nanoelectronics (IMEN) UKM.

Day one of the conference had three keynote speakers: Dr. MK. Radhakrishnan, of NanoRel delivered a talk entitled "*Analysis Challenges and Interface Physics in Silicon Nanodevices,*" followed by Dr. Burhanuddin Yeop Majlis, the Director of IMEN, UKM, who delivered a speech entitled *"MEMS and Lab on Chip: Interfacing Macro to Nano World."* The session ended with a keynote by Dr. Mehmet Ertugrul from Ataturk University, Turkey, entitled "*Artificial Pinning Centers for Superconducting Microwave Resonators."*

Keynote talks on the second day of the conference began with Dr. Albert Chin, of National ChiaoTung University, delivering his speech entitled *"Low Power Green Electronic Devices*," followed by Dr. Hei Wong of City University Hong Kong, with a speech entitled *"Silicon Photonics*

Participants of RSM 2013 at Langkawi, Malaysia

for Microelectronic On-Chip Optical Interconnects." The last two keynote speakers were Dr. Uda Hashim, Director of the Institute of Nano Electronic Engineering (INEE) UniMAP speaking on *"Fabrication and Characterization of Polysilicon Nanogap Device for DNA Hybridization Detection,"* and Dr. Masuri bin Othman, Director of Commercialization from the Ministry of Science, Technology and Innovation (MOSTI) Malaysia, speaking on "*An Overview of Innovation Ecosystem in Malaysia.*"

IEEE EDS DL speaker Dr. Paul Berger(first row, 4th from left) and participants at Universiti Putra Malaysia

ED Malaysia

–by P Susthitha Menon and Maizatul Zolkapli

The IEEE ED Malaysia Chapter organized three technical talks including two EDS Distinguished Lectures and two DL Colloquium during the 3rd quarter of 2013. Apart from these, the Chapter's own regional conference, RSM 2013, was successfully held at Langkawi, Malaysia. Reports on the DL Colloquium and RSM conference are given separately.

The two Distinguished Lectures included Dr. Arokia Nathan of Cambridge, giving a talk on "*Large Area Electronics and Mobile Energy"* at Universiti Kebangsaan Malaysia (UKM) on July 18, 2013, a DL by Dr. Paul Berger of Ohio State University, USA, on "*A Case Study of Polymer-Fullerene Derivative Bulk Heterojunction Photovoltaics"* at Universiti Putra Malaysia (UPM) on August 14, 2013 and a Technical Talk on "*Impact of Variability Issues in CMOS processes on design of Circuits in Nano-era (sub 45 nm)"* by Dr. Arun Chandorkar of IIT Bombay, India on August 29, 2013.

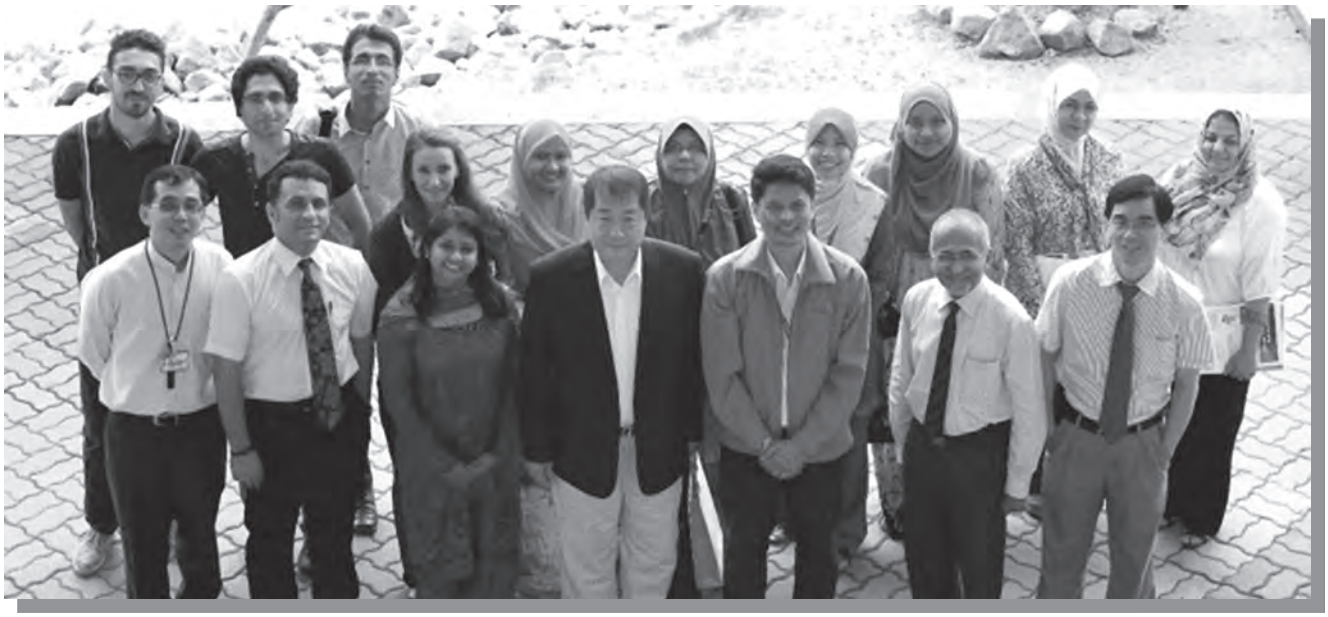
A Social Event called Buka-Puasa (Breaking of Fast during the holy month of Ramadan) was held on July 15, 2013, by the IEEE EDS Malaysia Chapter at Residence Hotel@ UNITEN, where the Chapter committee reviewed the activities of the year. For the past 3 years, the ED Malaysia Chapter has been presenting the best Final Year Project (FYP) awards to micro and nanoelectronic engineering undergraduate students at local public universities. Three recipients of this year are: 1. Ms. Oh Soo Ling of Universiti Kebangsaan Malaysia for the project thesis *"Design of Ring-based Injection-Locked Frequency Divider in 0.18-micron CMOS for Active RFID applications"*, 2. Ms. Arina Diyana binti Arifin of International Islamic University of Malaysia (UIA) for the project thesis *"Analysis of Radiation Effect on the current-voltage and capacitance-voltage properties of Si and GaP diodes"* and 3. Ms. Nurfarhana binti Mohd Ariffin, of Universiti Sains Malaysia (USM), for the project, *"Fabrication and characterization of zinc-doped GaN thin films using spin coating methods."* Recipients get monetary benefits of one year free IEEE student memberships and certificates.

The ED Malaysia Chapter committee met with IEEE EDS Region 10 SRC Vice-Chair, Dr. MK Radhakrishnan on September 26, 2013, to discuss ways of strengthening Chapter activities. Among the major items discussed and activities planned are to increase membership through various educational events at different electronic industry locations, elevation to senior membership, formation of student chapters wherever potential exists with proper guidance, publicity and expansion of annual conferences, and organizing workshops to attract members from industry.

Report on EDS Mini-Colloquia Organized by the ED Malaysia Chapter

–by P Susthitha Menon and Mohd Nizar Hamidon

The IEEE ED Malaysia Chapter organized two EDS Distinguished Lecturer (DL) events September 23–24,



EDS Distinguished Lecturers: Dr. Albert Chin, Dr. MK Radhakrishnan and Dr. Hei Wong, with researchers from UPM and UKM

2013. On September 23rd the DL program at Universiti Putra Malaysia (UPM), Kuala Lumpur had three DL speakers: Dr. Albert Chin, Distinguished Professor of National Chiao Tung University, Taiwan; Dr. Hei Wong of City University, Hong Kong and Dr. MK Radhakrishnan of NanoRel Technical Consultants, Singapore. Dr. Mohd Nizar Hamidon, the Chapter Chair presided and introduced the speakers. The first DL by Dr. Albert Chin was on *"Low Power Green Electronics;"* Dr. Hei Wong's talk on *"Silicon Photonics for Microelectronic Op-Chip Optical Interconnects;"* and Dr. Radhakrishnan's introduction of the ED Society and its benefits to members followed by his technical talk on *"Physical Analysis of Silicon Nanodevice Interfaces."* The talks were attended by researchers and graduate students from both UPM and Universiti Kebangsaan Malaysia (UKM).

The second EDS DL Program, held on September 24th, at Universiti Malaysia Perlis (UniMAP) at Perlis, was hosted by Dr. Zaliman Sauli. Dr Albert Chin's lecture was on Low Power Green Electronics followed by Dr. Hei Wong's talk on Silicon Photonics for Microelectronic Op-Chip Optical Interconnects. A good number of research fellows and graduate students attended the DL programs at both locations. The mini-colloquia was organized and funded by the ED Malaysia Chapter as a service to its members and professionals in the Society.

ED HITK Student Chapter & ED Calcutta

–by Atanu Kundu and Chandan Sarkar

The ED HIT Student Chapter and ED Calcutta Chapter jointly organized a Distinguished Lecture on *"Convergence of Nanoelectronics, Nanotechnology and Information Technology; Future Challenges"* by Prof. Durga Misra, of New Jersey Institute of Technology, USA, on August 14, 2013, at Heritage Institute of Technology, Calcutta. A total of 120 students attended the talk along with faculty members from various engineering colleges. The event was extremely successful in bringing together students from electronics and communication engineering departments and providing them an opportunity to interact with experts.

A tutorial on *"Next Generation 2-D Channel Material based MOSFETs: Overview and Simulation Tools"* was jointly organized by Heritage Institute of Technology, Kolkata, the IEEE ED HITK Student Chapter, and the ED Calcutta Chapter on September 4, 2013. The tutorial was given by Dr. Amretashis Sengupta from Indian Institute of

Prof. Durga Misra giving his Distinguished Lecture to the attendees at HITK, Calcutta

Science (IISc), Bangalore, India. About 110 students participated in the event, which was beneficial to the graduate students.

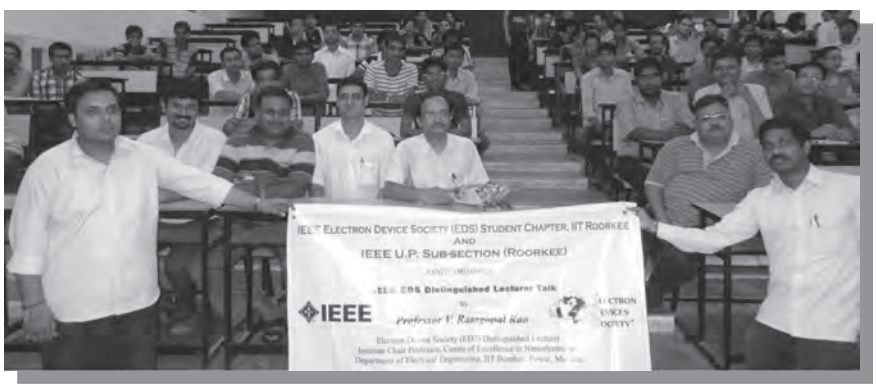
ED IIT Roorkee Student Chapter

–by Pankaj Pal and S Manhas

The ED IIT-Roorkee Student Chapter organized two Distinguished Lectures. Dr. M. Jagadesh Kumar, NXP (Philips) Chair Professor at IIT-Delhi gave a lecture on *"Steep Sub-threshold Green Transistors: Will they take over the conventional silicon CMOS?"* on August 28, 2013. His lecture covered a broad range of novel devices on current interest and produced lively and interactive discussions.

On August 30th, the chapter was honored to host another DL entitled "Multi-disciplinary Approach to Product Development: Opportunities & Challenges" by Prof. Dr. V. Ramgopal Rao, Institute Chair Professor, and Chief Investigator for the Centre of Excellence in Nanoelectronics at IIT-Bombay and EDS Region 10 SRC Vice-Chair. Prof. Rao discussed the latest developments, challenges and possible research opportunities in the field of MEMS and Sensors. His lecture began with a brief introduction to the IEEE Electron Devices Society. Both lectures were attended by more than 120 students, research scholar and professors.

Prof. Jagadish Kumar (seated, first row center) with professors and research students after the DL



Prof. Ramgopal Rao and participants of the DL

ED NIST Student Chapter, Berhampur

–by Ajit Kumar Panda

The ED NIST Student Chapter organized a four week Summer Training course in June, for its members on VLSI and its practices. The program was conducted for fourth semester students to learn and introduce VLSI Design and Device Processing. The program was conducted by the VLSI faculty team of NIST.

A workshop on *"VLSI Signal Processing,"* was organized by the Chapter on September 10–11, 2013. The workshop lecture was delivered by Prof. R. P. Panda of VSSUT, Burla, India. He emphasized how the Vedic Mathematics can be implemented using Signal Processing techniques and how to implement the same in VLSI Chip design. The program was attended by EDS student members.

Participants of summer training course organized by the ED NIST Student Chapter

Participants of the VLSI Signal Processing workshop by the ED NIST Student Chapter

Dr. Shen Chen (middle) with the audience after the talk

REL/CPMT/ED Singapore

–by Xing Zhou and Yeow Kheng Lim

The REL/CPMT/ED Singapore Chapter organized a technical talk on July 17, 2013, by Dr. Shen Chen from Cogenda Pte., Ltd. Dr. Shen's talk entitled, "*Radiation Effects in Semiconductor Devices and the Fully-Physical Simulation of Single-Event Effects,*" attracted lots of interest from students and attendees from local industry.

The flagship event of the Chapter, the IEEE International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA), held its 20th conference in Suzhou, China, July 15–19, 2013. IPFA 2013 was jointly organized by the IEEE Nanjing Section ED/SSC Chapter and the IEEE REL/CPMT/ED Singapore Chapter (report is given separately). The IPFA 2014 conference will be held in Singapore from June 30 to July 4, 2014 and details can be obtained at: http://ieee-ipfa.org/

~M.K. Radhakrishnan, Editor

ED Japan

–by Akira Toriumi

Our annual IRPS 2013 Report Meeting was held at the University of Tokyo, Tokyo, July 25th. Dr. M. Sato, Toshiba gave a general review of IRPS 2013, which was held in April. Dr. K. Kobayashi, Kyoto Institute of Technology, reviewed the topics on circuit reliability and aging simulation and H. Matsuyama from Fujitsu Semiconductor, reviewed the topics on BEOL reliability. Following the topic reviews, eight selected papers from the conference were presented by their authors: C. Ma, Hiroshima University; Y. Yonamoto, Hitachi; A. Yonezawa, Tohoku University; S. Kudoh, Renesas Electronics; T. Uemura, Fujitsu Semiconductor; K. Miyachi, Chuo University; S. Fujii, Toshiba; and K. Joguchi, Chuo University. More than 60 attendees from the academic and corporate communities enjoyed the discussions on the latest device reliability issues.

ED Kansai

–by Michinori Nishihara

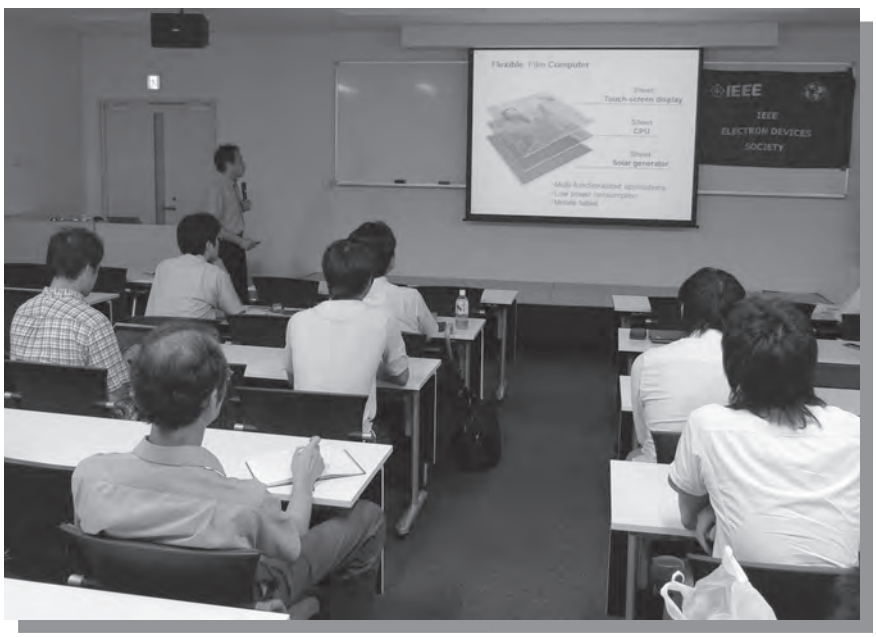
The ED Kansai Chapter held a Technical Meeting on July 29, 2013 at Osaka Center of Josho Gakuen, Osaka, Japan. Two prestigious lecturers were invited and their talks attracted 30 attendees.

The first speaker, Prof. Yukiharu Uraoka of Nara Institute of Science and Technology (NAIST), gave a lecture entitled, *"Future Display led by Oxidized Transparent Material."* Prof. Uraoka reviewed the most recent development statuses of oxide TFTs, motivated by the continuing requirement towards larger size LCD displays. High electron mobility is required for such large displays. Oxide TFTs, especially the one known by IGZO, show better mobility than a-Si:H TFTs and are getting much attention from both academia and industry. He also explained a collaboration scheme between academia and industry.

Dr. Tohru Mogami

IRPS 2013 Report Meeting at the University of Tokyo, on July 25, 2013

Attendees of the ED Kansai Chapter Technical Meeting



Prof. Yukiharu Uraoka

The second lecturer, Dr. Tohru Mogami of Photonics Electronics Technology Research Association (PETRA), gave his talk entitled, *"Si-LSI Innovations and Challenge."* Before explaining development trends of various FETs, he discussed a recent difficult situation of Japanese semiconductor companies. Based on his industry background, he gave his ideas on why it happened and how to improve the situation. His lecture was very thought provoking and encouraged young students to pursue their career.

The next event hosted by the ED Kansai Chapter will be the IEDM 2013 feedback meeting, scheduled for January 2014. Please check our chapter's website for more details: http://www.ieee-jp.org/section/kansai/chapter/eds/.

~ Kuniyuki Kakushima, Editor

EDS MEETINGS CALENDAR
(As of 06 November 2013)

The complete EDS Calendar can be found at our web site:
http://eds.ieee.org. please visit.

24 Mar - 27 Mar 2014
2014 International Conference on Microelectronic Test Structures (ICMTS)
Conf Record :32659
Location: Udine , Italy
Contact : Francesco Driussi
Tel : +39 0432 558295
Fax : +39 0432 558251
E-mail: francesco.driussi@uniud.it
Deadline : 13 Jan 2014
www : http://icmts2014.uniud.it

18 Apr - 18 Apr 2014
2014 IEEE Workshop On Microelectronics And Electron Devices (WMED)
Conf Record :32556
Location: Boise ID , USA
Contact : Jaydeb Goswami
Tel :
Fax :
E-mail: jgoswami@micron.com
Deadline : 17 Feb 2014
www : http://www.ewh.ieee.org/r6/boise/wmed2014/WMED2014.html

22 Apr - 24 Apr 2014
2014 IEEE International Vacuum Electronics Conference (IVEC)
Conf Record :20241
Location: Monterey CA , USA
Contact : Mark Goldfarb
Tel : 212-460-9700
Fax :
E-mail: mgoldfarb@pcm411.com
Deadline :
www : http://

28 Apr - 30 Apr 2014
2014 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)
Conf Record :32546
Location: Hsinchu , Taiwan
Contact : Jenny Lin
Tel : +886 3-5916705
Fax : +886 3-5820221
E-mail: vlsitsa@itri.org.tw
Deadline : 31 Oct 2013
www : http://vlsitsa.itri.org.tw/

28 Apr - 30 Apr 2014
2014 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)
Conf Record :32530
Location: Hsinchu , Taiwan
Contact : Elodie Ho
Tel : +886-3-5919039
Fax :
E-mail: elodieho@itri.org.tw
Deadline : 31 Jan 2014
www : http://vlsidat.itri.org.tw/

08 Jun - 13 Jun 2014
2014 IEEE 40th Photovoltaic Specialists Conference (PVSC)
Conf Record :21196
Location: Denver CO , USA
Contact : Richard R. King
Tel : +1 818 838 7404
Fax : +1 818 838 7474
E-mail: rking@spectrolab.com
Deadline : 26 May 2014
www : http://www.ieee-pvsc.org/PVSC40

08 Jun - 09 Jun 2014
2014 Silicon Nanoelectronics Workshop (SNW)
Conf Record :32907
Location: Honolulu HI , USA
Contact : Simon Deleonibus
Tel : +33 673518545
Fax :
E-mail: simon.deleonibus@cea.fr
Deadline :
www : http://

10 Jun - 12 Jun 2014
2014 IEEE Symposium on VLSI Technology
Conf Record :18214
Location: Honolulu HI , USA
Contact : Phyllis Mahoney
Tel : +1 301 527 0900
Fax : +1 301 527 0994
E-mail: phyllism@widerkehr.com
Deadline :
www : http://www.vlsisymposium.org

15 Jun - 17 Jun 2014
2014 20th Biennial University/Government/Industry Micro/Nano Symposium (UGIM)
Conf Record :32966
Location: Cambridge MA , USA
Contact : Eric Martin
Tel : +1 617-495-3161
Fax :
E-mail: emartin@cns.fas.harvard.edu
Deadline : 30 May 2014
www : http://www.cns.fas.harvard.edu/UGIM2014/index.php

15 Jun - 19 Jun 2014
2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)
Conf Record :20170
Location: Waikoloa HI , USA
Contact : Don Disney
Tel : +1 408 684 5223
Fax :
E-mail: ispsd.disney@gmail.com
Deadline : 08 Mar 2014
www : http://www.ispsd2014.com

09 Sep - 11 Sep 2014
2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)
Conf Record :32888
Location: Yokohama , Japan
Contact : Akira Hiroki
Tel : +81-75-724-7419
Fax :
E-mail: hiroki@kit.ac.jp
Deadline :
www : http://sites.google.com/site/sispad2014/

14 Sep - 17 Sep 2014
2014 IEEE Custom Integrated Circuits Conference - CICC 2014
Conf Record :18693
Location: San Jose CA , USA
Contact : Melissa Widerkehr
Tel : +1 301 527 0900
Fax : +1 301 527 0994
E-mail: melissaw@widerkehr.com
Deadline :
www : http://www.ieee-cicc.org

28 Sep - 01 Oct 2014
2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM
Conf Record :31342
Location: Chicago IL , USA
Contact : Catherine Shaw
Tel : 404-385-3555
Fax :
E-mail: Catherine.Shaw@pe.gatech.edu
Deadline : 18 Jul 2014
www : http://ieee-bctm.org/

29 Sep - 03 Oct 2014
2014 25th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF)
Conf Record :32961
Location: Berlin , Germany
Contact : Jasmin Kayadelen
Tel : +49 69 6308275
Fax : +49 69 6308144
E-mail: jasmin.kayadelen@vde.com
Deadline : 06 Jun 2014
www : http://www.esref2014.org

06 Oct - 09 Oct 2014
2014 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)
Conf Record :33072
Location: San Francisco CA , USA
Contact : Joyce Lloyd
Tel : 818-795-3762
Fax : 818-855-8392
E-mail: joyce@imf.la
Deadline :
www : http://http://s3sconference.org/

18 May - 21 May 2014
2014 IEEE 6th International Memory Workshop (IMW)
Conf Record :32432
Location: Taipei , Taiwan
Contact : Pei-Ying Du
Tel : +886955-986-685
Fax : +8863-578-9087
E-mail: pennydu@mxic.com.tw
Deadline :
www : http://

19 May - 21 May 2014
2014 25th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)
Conf Record :32974
Location: Saratoga Springs NY , USA
Contact : Margaret Kindling
Tel : +1-202-393-5552
Fax :
E-mail: mkindling@semi.org
Deadline : 28 Apr 2014
www : http://www.semi.org/asmc2014

20 May - 23 May 2014
2014 IEEE Internatioal Interrconnect Technology Conferencei/Advanced Metallization Conference (IITC/AMC)
Conf Record :32991
Location: San Jose CA , USA
Contact : Wendy Walker
Tel : +1-301-527-0900
Fax :
E-mail: wwalker@widerkehr.com
Deadline : 01 Feb 2013
www : http://www.his.com/~iitc

27 May - 30 May 2014
2014 International Conference on electron, Ion, and Photon Beam Technology and Nanofabrication (EIPBN)
Conf Record :32742
Location: Washington DC , USA
Contact : Theodore Fedynyshyn
Tel : +1-781-981-7811
Fax : +1-781-981-4983
E-mail: fedynyshyn@ll.mit.edu
Deadline : 31 Jul 2014
www : http://eipbn.org/

31 May - 05 Jun 2014
2014 IEEE International Reliability Physics Symposium (IRPS)
Conf Record :20379
Location: Waikoloa HI , USA
Contact : David Barber
Tel : +1 828 898 7001
Fax : +1 828 898 6375
E-mail: dbarbsta@aol.com
Deadline :
www : http://www.irps.org

18 Jun - 20 Jun 2014
2014 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)
Conf Record :32286
Location: Chengdu , China
Contact : Zhiwei Liu
Tel : +86-28-83201281
Fax :
E-mail: ziv_liu@hotmail.com
Deadline : 31 Mar 2014
www : http://www.edssc2014.com

22 Jun - 25 Jun 2014
2014 72nd Annual Device Research Conference (DRC)
Conf Record :32941
Location: Santa Barbara CA , USA
Contact : Ioannis Kymissis
Tel : 3478500235
Fax :
E-mail: johnkym@ee.columbia.edu
Deadline : 15 Apr 2013
www : http://www.drc.ee.psu.edu/

28 Jul - 31 Jul 2014
2014 IEEE International Nanoelectronics Conference (INEC)
Conf Record :31843
Location: Sapporo , Japan
Contact : Kazuhiko Endo
Tel : +81-29-861-3857
Fax :
E-mail: endo.k@aist.go.jp
Deadline : 31 May 2014
www : http://

05 Aug - 07 Aug 2014
2014 Lester Eastman Conference (LFE)
Conf Record :32909
Location: Ithaca NY , USA
Contact : Pane Chao
Tel : 6038856695
Fax :
E-mail: pane.chao@baesystems.com
Deadline : 22 Aug 2014
www : http://www.leconf.com

01 Sep - 05 Sep 2014
2014 29th Symposium on Microelectronics Technology and Devices (SBMicro)
Conf Record :33078
Location: Aracaju , Brazil
Contact : Edward David Moreno
Tel : +55 79 9198-4939
Fax :
E-mail: edwdavid@gmail.com
Deadline : 01 Jun 2014
www : http://www.sbmicro.org.br/sbmicro

13 Oct - 14 Oct 2014
INTERNATIONAL CONFERENCE ON COMMUNICATION & NANO TECHNOLOGY
Conf Record :31570
Location: CHENNAI , India
Contact : Arun prasad
Tel : +919865413635
Fax :
E-mail: pgsrtswj@gmail.com
Deadline : 06 Sep 2013
www : http://WWW.ICCNT-ECE.ORG

19 Oct - 22 Oct 2014
2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSISC)
Conf Record :31991
Location: San Diego CA , USA
Contact : Douglas McPherson
Tel : +1 613-670-3371
Fax :
E-mail: dmcphers@ciena.com
Deadline : 25 Jul 2014
www : http://www.csics.org

10 Dec - 13 Dec 2014
2014 IEEE 45th Semiconductor Interface Specialists Conference (SISC)
Conf Record :31578
Location: San Diego CA , USA
Contact : Alex Demkov
Tel : +1 512 471 8560
Fax :
E-mail: demkov@physics.utexas.edu
Deadline : 20 Aug 2014
www : http://www.ieeesisc.org/

11 Dec - 19 Dec 2014
2014 IEEE International Electron Devices Meeting (IEDM)
Conf Record :11149
Location: San Francisco CA , USA
Contact : Ms. Phyllis W. Mahoney
Tel : +1 301 527 0900 (Ext.103)
Fax : +1 301 527 0994
E-mail: phyllism@widerkehr.com
Deadline :
www : http://

BoG Meeting Recap and New EDS President Elect!

(continued from page 1)

documents will be provided to all members once the IEEE Technical Activities Board has approved them. So please be on the lookout for these soon.

Of course, the most important event of the December BoG meeting is the annual elections. This year the BoG members voted for the new class of 7 Members-at-Large, Secretary, Treasurer, and President-Elect. All 25 full-voting BoG members were present for the election. The results are as follows:

Members at Large: Arturo Escobosa, Ru Huang, Leda Lunardi, Mikael Ostling, MK Radhakrishnan, Jacobus Swart, and Xing Zhou.
Secretary: Fernando Guarin
Treasurer: Ravi Todi
President-Elect: Samar Saha

"As President of EDS, I will execute my commitment to EDS and nurture our volunteers to contribute to their fullest extent to grow EDS in all key areas of endeavors."

Our sincere thanks to all those who took part in this year's election and congratulations to all the 2014 electees!

Lastly, this meeting brings a close to Paul Yu's tenure as EDS President. In his parting remarks to the over 1,000 attendees of the IEDM plenary Paul said that his time as EDS President is a great honor he will forever cherish and he extended his full support to his successor Albert Wang. We offer Paul our deepest appreciation for his visionary leadership and unwavering dedication to EDS and join him in wishing Albert all the best in his tenure as EDS President.